Solid State Lighting Program
Final Report

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Epitaxial Growth of GaN-based LEDs on Simple Sacrificial Substrates

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1. Executive Summary

The objective of this project is to produce alternative substrate technologies for GaN-based LEDs by developing an ALD interlayer of Al_2O_3 on sacrificial substrates such as ZnO and Si. A sacrificial substrate is used for device growth that can easily be removed using a wet chemical etchant leaving only the thin GaN epi-layer. After substrate removal, the GaN LED chip can then be mounted in several different ways to a metal heat sink/reflector and light extraction techniques can then be applied to the chip and compared for performance. Success in this work will lead to high efficiency LED devices with a simple low cost fabrication method and high product yield as stated by DOE goals for its solid state lighting portfolio.

This work required development of growth techniques for substrates other than sapphire, such as ZnO and Si. Growth of GaN on ALD/ZnO had many promising breakthroughs, but after extensive experimentation it was found that the MOCVD tool at this time is not able to grow device quality films on ZnO. Therefore the majority of recent work was directed toward growth on ALD/Si. MOCVD growth processes have been developed for high-quality GaN on silicon substrates using an ALD-grown Al_2O_3 interlayer to improve material quality. The data obtained from growth on silicon is approaching typical values reported for GaN on sapphire. This is a significant improvement over 40% for some metrics such as x-ray linewidth to that previously reported in the literature. GaN-based LEDs were grown using the GaN growth process developed in the early phase of this work. These devices showed substantial improvement of performance characteristics compared with the LED devices on bare Si. A comparison of similar LEDs on GaN and ALD-Al_2O_3/silicon reveals several points that show continued promise for high efficiency GaN-based LEDs on silicon substrates:

1) Similar IQE (within error) for devices on Si and sapphire (IQE_{Si} = 33%; $IQE_{Sapphire}$ = 37%)
2) Enhanced emission wavelength stability for varying drive currents for devices on Si compared to those on sapphire.
3) Reduction of current droop at high drive currents for LEDs on silicon compared to those on sapphire, as evidenced by L-I measurements.

These properties show great promise for high-efficiency GaN-based LEDs on silicon substrates. Additionally, silicon is less expensive than sapphire per unit area by a factor of four. A full industrial based cost of ownership model shows that using a silicon substrate results in a reduction of ~33% in yielded cost of LED wafers ($28.26 to $18.84), *which is a significant cost reduction as required in the DOE SSL Multi-Year Program Plan (MYPP).* It is found, however, that the Si substrate removal process by wet etching and transfer of GaN based devices to copper carrier or other heat sinks is still posing challenges and would need further investigation in the future.

2. Metrics

The gate metrics for success in Tasks 1 and 2 of this project are related to material quality and initial device performance. The gate metrics in Task 3 are related to removal of the sacrificial substrate via a simple acid wet etch process and mounting the LEDs on to a metal heat-sink, with the inclusion of an evaporated metal contact/reflector scheme in between, followed by light extraction techniques. These metrics include quantities such as internal quantum efficiency (IQE), external quantum efficiency (EQE), and light extraction efficiency. The most fundamental of these quantities is IQE, which is defined as the ratio of the number of photons emitted from the active region to the number of electrons injected into the active region. The main focus of this project over the period has been the improvement of material quality and consequently the measurement and improvement of IQE for GaN-based blue and green emitters as defined in the project gate metrics.

2.1 Stage-Gate Analysis

Gate metrics for Tasks 1 and 2 in this project are related to material quality and initial results from GaN-based devices on sacrificial substrates, respectively. Gate metrics for Task 1 are shown in Table 1. All the gate metrics for Task 1 were met. These metrics are related to material quality and provide a foundation on which to pursue high-quality devices. A summary of the material properties of GaN on Si that have been achieved in this work in response to the metrics set in Task 1 are shown in Table 2. Material quality exceeded gate metrics for structural and optical properties.

Table 1: Task 1 gate metrics.

Metrics			
	Structural	**Optical**	**Electrical**
Task 1	***XRD*** **(002) FWHM ≤ 500 arcsec**	***RT-PL*** **FWHM ≤ 0.4 eV**	***Hall Effect*** $n \leq 2.0 \times 10^{18}$ cm^{-3} $\mu > 350$ cm^{2}V^{-1}s^{-1} ***SIMS*** Conc.$_{(C, O)} \leq 10^{18}$cm^{-3}

Table 2: Summary of GaN properties on Si(111).

	XRD		PL		AFM
	(002) FWHM (arcsec)	(102) FHWM (arcsec)	FWHM (meV)	BL/YL	RMS roughness (Å)
HT-AlN buffer on Si	549.3	977.5	49.3	5.396	5.67
LT-AlN interlayers on Si	436.8	1041.9	46.9	5.521	3.99
5nmAl_2O_3/Si	378.6	849.5	46.5	7.395	3.93
10nm Al_2O_3/Si	433.9	1344.6	47.7	4.497	5.65
20nm Al_2O_3/Si	416.6	740.1	43.4	28.223	3.70

This work provides a foundation on which to build a device technology that could be competitive with GaN on sapphire. Gate metrics for Task 2 are related to initial device performance, Table 3. The gate metrics for X-ray, Hall concentration, and $V_{turn\text{-}on}$ were all met

for Task 2. These metrics are based on typical values for GaN-based LEDs on sapphire. While reports of GaN-based LEDs with much higher efficacy and efficiency characteristics have been published, this work is aimed at showing performance of devices on Si that is comparable to similar devices on sapphire. These metrics provided a reasonable baseline to demonstrate this equality of performance.

Table 3: Task 2 gate metrics.

Metrics			
	Structural	**Optical**	**Electrical**
Task 2	***XRD*** **(002) FWHM ≤ 450 arcsec**	***LED Spectrum*** **> 10 lumens/Watt (350µm x 350µm)**	***Hall Effect*** **n ~ 1.0 x10^{17} cm^{-3}** **µ > 450 $cm^2V^{-1}s^{-1}$** ***I/V Curve*** **$V_{turn-on}$ < 4.2V @ 20mA** **120 mW (4V @ 30 mA)** ***L/I Curve*** **IQE > 30%**

Crack-free GaN-based LEDs have been fabricated on both Si(111) and sapphire substrates using the growth process developed in Task 1. GaN-based devices were fabricated on both bare Si and Al_2O_3/Si. It is clear that the ALD-Al_2O_3 interlayer developed in Task 1 significantly reduces cracking density, and crack-free devices were fabricated on Al_2O_3/Si substrates, Figure 1(a). Devices fabricated on sapphire are shown for comparison, Figure 1(b).

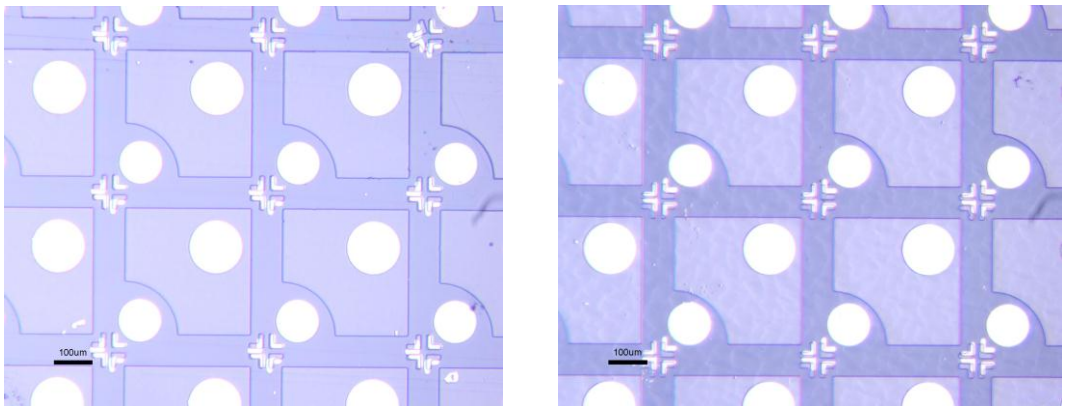


Figure 1: (a) Crack-free GaN-based LEDs fabricated on Si(111) substrates, (b) GaN LEDs fabricated on c-Al_2O_3 substrates.

These results provide a solid foundation on which to build a Si substrate technology for MOCVD growth of GaN-based LEDs. Later work was focused on the measurement and improvement of the IQE of GaN-based LEDs on Si as well as the substrate removal process. IQE is the most fundamental quantity related to LED efficiency, and improvements in IQE will make a significant contribution to the SSL Multi-Year Program Plan (MYPP) as well as to the current state of the art.

2.2 Multi-Year Program Plan (MYPP)

The metrics for success in this project have been updated to reflect the significant advances that have been made in the field of solid state lighting (SSL) in the past few years. Relevant barriers to the use of LEDs in general lighting applications, as listed in the U.S. Dept. of Energy SSL MYPP, along with projected values for the given metric are shown in Table 4 [1]. The major barriers relevant to this project are cost, efficacy, and total lumen output.

Table 4: Barriers to the adoption of solid state lighting.

Barrier	***Metric***	***Projected Value***	
		2007	2010
Cost	$/klm	25	10
Luminous Efficacy	lm/W	120	160
Lumen Output	Total lm	N/A	

These barriers are related to two major issues: efficiency and cost. MYPP priorities for LED Core Technology, which are aimed at overcoming these barriers, are shown in Table 5. The relation between the priorities in Table 5 is shown in Equation 1,

$$\eta_{ext} = \chi \cdot \eta_{\text{int}} \qquad (1)$$

where η_{ext} is external quantum efficiency (EQE), χ is light extraction efficiency, and η_{int} is internal quantum efficiency (IQE). It is clear that EQE is dependent on the two more fundamental quantities, IQE and light extraction efficiency, and an improvement in EQE can only result from an improvement in one of these two quantities. The focus of this project is the use of alternative substrate technologies to improve device IQE while developing simpler processing methods – such as substrate removal by wet etching – that allow for increased light extraction efficiency, thus improving overall LED performance. An additional advantage of Si is the reduced substrate cost, which is a significant fraction of the cost of operating an MOCVD system and has a significant effect on final device cost.

Table 5: MYPP LED Core Technology research priorities relevant to this project.

Priority	***Task***	***Target Value***		
			2007	2015
2008 Priority	1.1.2 Improve IQE (η_{int})	Green	20%	90%
		Blue	80%	90%
Later Priority	1.2.1 Improve EQE (η_{ext})	50%		80%
Later Priority	1.2.2 Improve LEE (χ)	80%		90%
Long Term	1.1.1 Large-area substrates	N/A		

The gate metrics for Task 2 are chosen to address the issue of efficiency, while the objective of the project – the development of Si as a substrate technology for GaN epitaxy – addresses the issue of cost and development of large-area substrates. The most important gate metric related to device performance is IQE, as it directly affects both the power efficiency and total light output of the device. The investigation of devices with different emission wavelengths is also important,

as IQE tends to be much higher in the blue spectral region (~450nm) than it is in the green region (500-550nm). A search on devices with a range of peak wavelengths will provide insight into the loss mechanisms that cause a decrease in IQE as well as methods to overcome these loss mechanisms. In this project, GaN-based LEDs spanning these two spectral regions have been grown on Si substrates by MOCVD and measured for IQE. ZnO has also been investigated as a substrate for GaN epitaxy, and results from this study are given in this report. However, more promising results have been obtained on Si, and so the majority of the device work included in this report was done using Si substrates.

2.3 Internal Quantum Efficiency Measurement

The transition from excited state to ground state can be either radiative (energy dissipation by emission of photon) or nonradiative (energy dissipation by emission of phonon). In an externally excited system, at thermal equilibrium, there is a competition between radiative and nonradiative recombination processes. Nonradiative recombination processes result in the emission of phonons, which correspond to a temperature increase in the sample and a decrease of luminescence intensity. The competition between these two processes determines the IQE of the LED. The total light output of an LED quantified as external quantum efficiency is determined by IQE and light extraction efficiency, as mentioned in Equation 1. The IQE relates to the material quality and the light extraction is more dependent on the device design.

The main issue [2] associated with achieving high IQE is carrier confinement. Increasing the indium percentage in $In_xGa_{1-x}N$ or narrowing the well width can achieve the localization of carriers in the quantum wells and improve the internal quantum efficiency. The other issue [3] is the piezoelectric polarization induced effects originating from strain due to lattice-mismatch.

The relative contribution of radiative decay processes is determined from quantum efficiency (q):

$$q = \frac{\text{Number of photons emitted}}{\text{Number of photons absorbe}} \quad (2)$$

The measurement of absolute efficiencies is difficult, owing to pitfalls in setup requirements and calibration procedures. A good indication of quantum efficiency is obtained by measuring relative quantum efficiency, done by comparison with a standard sample. Several other techniques to get an estimate of quantum efficiency are used. The most common is by measuring temperature dependent output luminescence of samples [4]. At low temperature the quantum efficiency can be assumed unity, as the phonon transition are temperature dependent and are frozen at low temperatures. This technique is widely used in solid-state lighting community. In this technique the temperature dependent photoluminescence spectra is integrated and normalized to the value obtained at low temperature (< 8 K). This is the approach used in this project.

2.4 Cost Advantages of Si Substrates

A cost of ownership model has been developed for current EMCORE E300 technology and new Applied Materials (AM) tool that is currently operational in TSMC (Epistar) in Taiwan. The Epistar/AM tool can grow on 52 wafers/growth run resulting in ~3150 wafers per week with an estimated cost of ~$28/wafer including the substrate. The cost per wafer for the E300 tool of $43.66 reduces to cost per wafer of $28.26 for the AM tool using similar variables. The estimated close cost of the epitaxial material is now close to the industry metric of about 1.5x the wafer cost. **Additional cost savings can now only be made with reduction in the cost of the**

substrate material. Using an equivalent cost per square inch for silicon results in a factor of four (4) reduction in the substrate costs. Table 6 summarizes costs associated with ownership and operation of an MOCVD production system. This full CoO model shows that using a silicon substrate results in a reduction of ~33% in yielded cost of LED wafers ($28.26 to $18.84).

Table 6: Cost of ownership of an MOCVD system for LED production.

System Process Wafer Size	**E300** **LED (Sapphire)** 2"	**AM (52 wafers)** **LED (Sapphire)** 2"	**AM (52 wafers)** **LED (Silicon)** 2"
Capital for basic system(s) ($)	$1,600,000.00	$3,000,000.00	$3,000,000.00
Facilitation costs ($)	**$160,000.00**	**$300,000.00**	**$300,000.00**
Total capital required ($)	**$1,760,000.00**	**$3,300,000.00**	**$3,300,000.00**
Time to depreciate (years)	7	7	7
Annual depreciation ($/year)	**$251,428.57**	**$471,428.57**	**$471,428.57**
Required floor space (sq. meter)	26.00	26.00	26.00
Cost per square meter ($/sq.m/month)	$30.00	$30.00	$30.00
Average Power required (kw.hr)	30.00	30.00	30.00
Cost per kilowatt hour ($/kw.hr)	$0.10	$0.10	$0.10
Number of operators required/system	0.50	0.50	0.50
Operator's Salary + Overhead ($/hr)	$15.00	$15.00	$15.00
Cost of epi materials ($/run)	$400.00	$600.00	$600.00
Operating Cost @ full utilization ($)	**$1,378,991.56**	**$2,032,966.58**	**$2,032,966.58**
Total Annual Operating Cost ($)	**$1,630,420.13**	**$2,504,395.15**	**$2,504,395.15**
For required number of systems			
CPWP @ full utilization	**$27.89**	**$15.65**	**$15.65**
CPWP @ user rate	**$27.97**	**$15.70**	**$15.70**
Cost of substrate wafer ($)	$15.00	$12.00	$3.00
Yielded cost of wafer ($)	**$15.70**	**$12.56**	**$3.14**
CPWP + Substrate @ full utilization	**$43.59**	**$28.21**	**$18.79**
CPWP + Substrate @ user rate	**$43.66**	**$28.26**	**$18.84**

3. **Work Summary**

Tasks in Year 1 focused on MOCVD growth of GaN on ZnO (0001) substrates using ALD-grown Al_2O_3 as a transition layer to prevent Zn and O diffusion and NH_3 etching of the ZnO substrate. Work in Year 2 has focused on the development of an MOCVD growth process for GaN on Si using an Al_2O_3 interlayer and on fabrication and testing of GaN-based LEDs on Si. Work in Year 3 was aimed at developing a low cost device fabrication and substrate removal process realized by wet etching after the transfer of GaN epilayer/devices on to a metal heat sink. There are four major aspects to this work. First, ALD-grown Al_2O_3 interlayers on Si were investigated. The crystallinity and surface morphology of these layers was studied. Second, an MOCVD growth process was developed for GaN thin films on bare Si. This process was then transferred to Al_2O_3 /Si substrates. Thirdly, GaN-based devices were fabricated on Al_2O_3 /Si substrates and measured for IQE. The devices on Al_2O_3 /Si were shown to have similar performance characteristics to comparable devices on GaN/sapphire templates. Finally, the Si substrate removal process by wet etching, deposition of anti reflection coating and GaN epilayer bonding to the copper substrate were investigated.

3.1 Year 1

The tasks in Year 1 focused on the MOCVD growth of high-quality GaN thin films on ZnO exhibiting good crystalline structure, optical activity, and good electrical properties. This was achieved by furnace annealing the ALD-Al_2O_3 layers to crystallize them prior to MOCVD growth. A series of GaN and InGaN growths were then completed on these ALD-Al_2O_3/ZnOsubstrates.

In previous work by the PI (Ferguson) an extensive study of GaN growth on bare ZnO was completed and in this work it was proposed to use ALD as a means to solve the issues related to growth on ZnO. For example, growth of GaN on bare ZnO showed cracks and peeling off of the epilayer due to Zn diffusion from ZnO and H_2 etching from NH_3. These issues were solved, but Zn diffusion did not allow for high quality GaN growth. A transition layer of Al_2O_3 was placed before the MOCVD growth in order to provide a protective layer and promote GaN growth. This layer also acts as a stabilizing layer when the sacrificial substrate is etched off.

Table 7: Summary of ALD growths.

ALD-Al_2O_3	**ALD Growths**		
Plane/Phase	**100°C**	**350°C**	**600°C**
2nm	**x**	**x**	
5nm	**x**	**x**	
10nm	**x**	**x**	
20nm	**x**		
30nm	**x**		
50nm	**x**		
60nm	**x**		
90nm	**x**	**x**	**x**
100nm	**x**		
200nm	**x**		

Table 8: Summary of ALD-Al_2O_3 annealing studies on ZnO.

ALD-Al_2O_3/ZnO	**N_2, 1100°C furnace annealing**															
Plane	**5nm Al_2O_3**			**10nm Al_2O_3**				**20nm Al_2O_3**				**50nm Al_2O_3**			
	15min	30min	60min	0min	5min	10min	20min	0min	10min	20min	40min	0min	20min	50min	100min
(110) Al_2O_3	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**
(113) Al_2O_3		**x**	**x**		**x**			**x**	**x**			**x**	**x**		
(024) Al_2O_3	**x**	**x**	**x**		**x**				**x**	**x**		**x**	**x**	**x**	
(306) Al_2O_3	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**

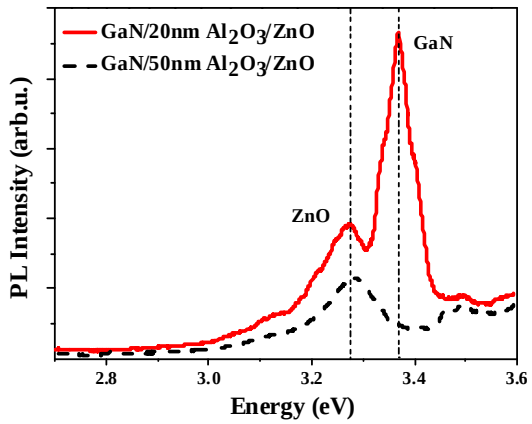


Figure 2: PL of GaN on ZnO with 20nm and 50nm Al_2O_3 transition layer.

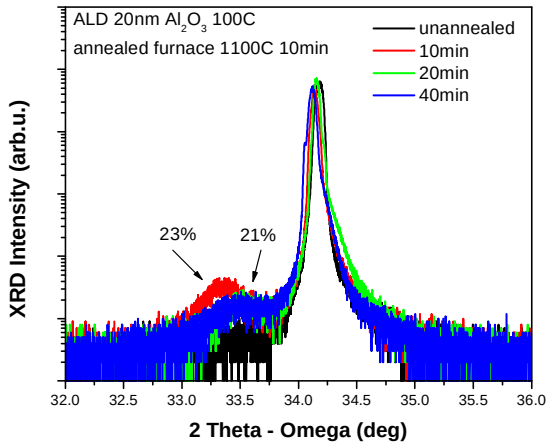


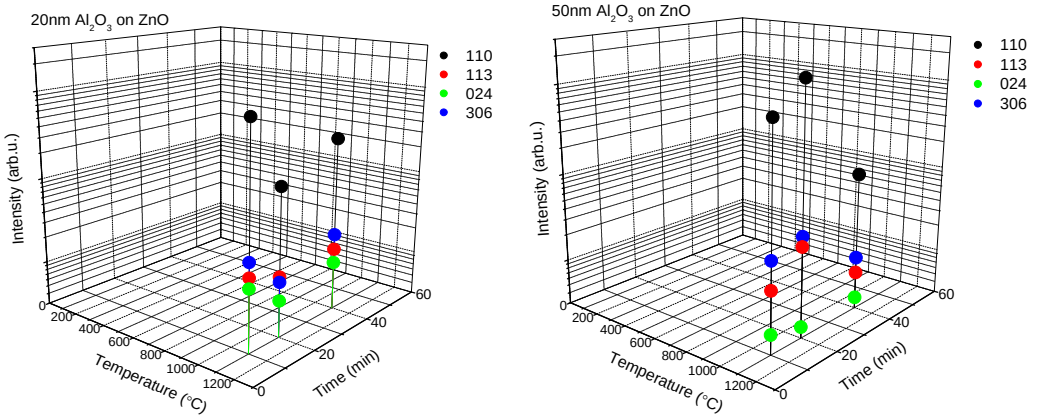
Figure 3: InGaN on ZnO for various annealed 10nm ALD-Al_2O_3 layers.

A systematic growth of ALD layers on both ZnO (and Si) have been investigated. The approach is to obtain enough empirical data and produce an empirical model to further optimize material growth and hence LED structures. A number of ALD samples have been grown as can be seen in Table 7. These ALD layers are initially amorphous and therefore the samples need to be annealed in order to form crystalline structures. RTA, *in-situ*, and furnace annealing have all been investigated. Furnace annealing was used in the end due to its clean environment from other chemicals and its ability to anneal for long periods at high temperatures of greater than 1000ºC. All samples were annealed at various temperatures ranging from 1100ºC to 1300ºC for various times of 5 to 100 minutes, see Table 8. These annealing studies were performed in order to understand the best crystallization of the amorphous ALD layer for growing GaN by MOCVD. One example is 20nm ALD-Al_2O_3 grown on a ZnO substrate and annealed at 1100ºC for 10, 20, and 40 minutes. The (110), (306), (113), and (024) planes of Al_2O_3 were formed on all the annealed samples but at various intensities. The un-annealed sample also showed the (110) and (306) peaks, and therefore shows that the Al_2O_3 layer might be polycrystalline after ALD growth.

GaN growths were done on the different annealed Al_2O_3/ZnO. The PL for the optimized GaN layer on Al_2O_3/ZnO showed a distinct GaN peak with a FWHM of 0.02eV, Figure 2. InGaN was also grown on different annealed Al_2O_3/ZnO substrates with various indium compositions including on un-annealed samples. One example is InGaN on 20nm Al_2O_3/ZnO, Figure 3. Only one significant InGaN peak is observed for 10 minutes annealing and weak InGaN peaks were found for the rest of the annealed samples. No InGaN peak was seen on the un-annealed sample. The intensity of this InGaN peak decreased with increasing annealing time. This case, for 20nm ALD-Al_2O_3 film demonstrates that the transition layer is a promising layer for heteroepitaxy growth of GaN and InGaN and thereby leading towards the feasibility of growing quality LEDs on a sacrificial substrate.

3.1.1 Annealing Studies of ALD-Al_2O_3/ZnO substrates

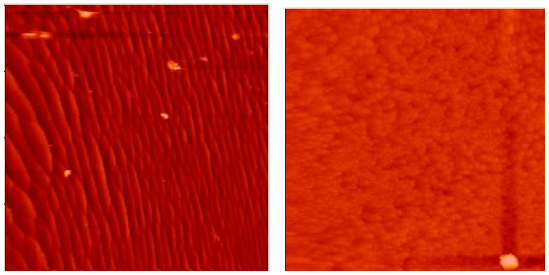
Al_2O_3 films of 20nm were deposited on ZnO substrates and then annealed at 10, 20, and 40 minutes at 1100ºC. HRXRD result showed the (002) and (004) peaks of the ZnO substrate. Additional peaks of interest were located at 38°, 44.5°, 52.5°, and 82°, which were assigned to the planes (110), (113), (024), and (306) of the α-Al_2O_3 phase from the JCPDS database for 10 minutes annealing. However, the (113), (024), and (306) planes decreased in intensity after 20



(a) (b)

Figure 4: HR-XRD results of (a) 20nm and (b) 50nm Al_2O_3 films deposited on ZnO substrates by ALD with different annealing conditions.

minutes of annealing. Furthermore, the (024) plane also decreased after 40 minutes of annealing. Therefore, the optimal annealing time at 1100ºC for crystallization may be at 10 minutes where the maximum number and highest intensity for the peaks can be obtained. A 3D image of the results is shown in Figure 4(a). The surface morphology of the as-deposited and post-annealed 20nm Al_2O_3 film was measured by AFM as seen in Figure 5. It can be seen that the surface of the as-deposited Al_2O_3 film has a terrace-like feature and excellent conformity, Figure 5(a). The root mean square (RMS) roughness of the as-deposited is about 1.6nm. Moreover, the RMS roughness increased to 3.5nm after 10 minutes annealing, Figure 5(b).



(a) (b)

Figure 5: Atomic force microscopy scans (10x10μm) of 20nm Al_2O_3 films deposited on ZnO substrates for (a) as-deposited and (b) after 10 minutes, 1100ºC annealing.

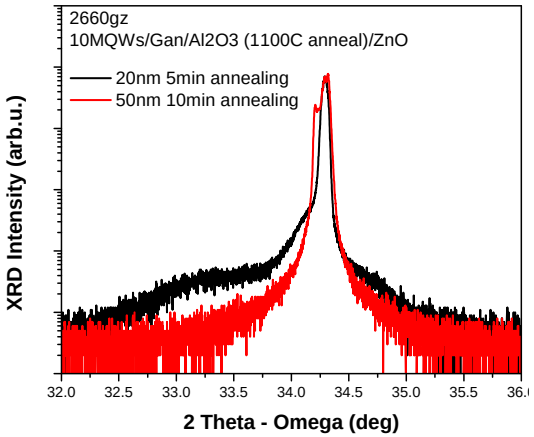
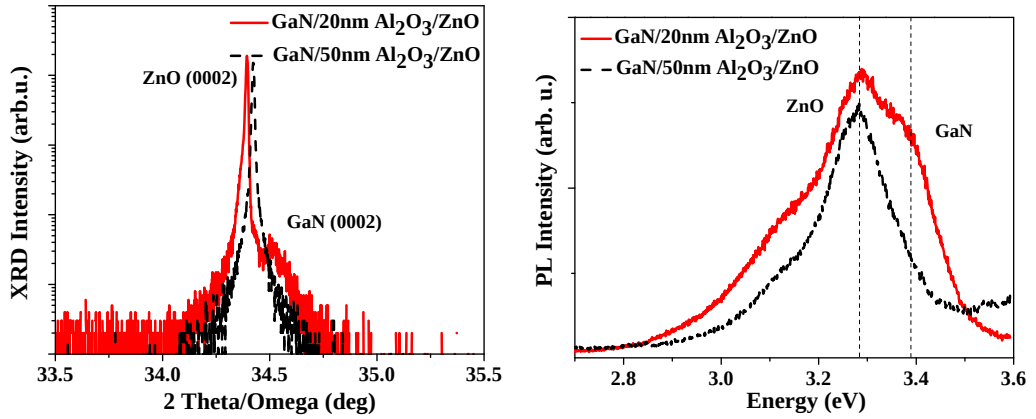


Figure 6: MQWs grown on ALD-Al_2O_3/ZnO.

HR-XRD was also measured on 50nm Al_2O_3 films for 10, 20, and 40 minutes at 1100ºC annealing, Figure 4(b). The 20 minutes annealed sample shows the planes relating to (110), (113), (024), and (306) of the α-Al_2O_3 phase, which are the same peaks shown for 20nm Al_2O_3 films after 10 minutes. However, the peak intensity of the (024) plane is significantly reduced. Moreover, the (024) plane disappears as the annealing time goes to 40 minutes. Note that the most peaks as well as highest intensity peaks show up at 20 minutes annealing. It is believed that 10 and 20 minutes annealing can improve the crystalline quality of 20 and 50nm as-deposited Al_2O_3 films as identified by HR-XRD.

3.1.2: Epitaxial Growth of GaN on ALD-Al_2O_3/ZnO Substrates

After the optimization of GaN layers on ALD/ZnO, the knowledge gained was applied it to MQWs on ALD/ZnO in order to move forward to growing LEDs. A baseline of InGaN/GaN 5MQWs was first grown on GaN templates to obtain the optimal recipe before transferring to



(a) (b)

Figure 7: (a) HRXRD 2θ/ω scan and (b) RT-PL spectra of GaN layers grown at 800ºC on 20 and 50nm annealed Al_2O_3/ZnO substrates by MOCVD.

growth on ALD-Al_2O_3/ZnO substrates. X-ray showed multiple distinct satellite peaks from the MQWs on GaN template. This optimized recipe led to the increase of 10MQWs (GaN/InGaN) grown on bare ZnO substrates in order to block the Zn/O diffusion from the ZnO substrate and enhance the band emission for subsequently grown epilayers. Following the MQWs, a 50nm GaN cap layer was added on top of the MQWs. Several additional approaches were performed as well in order to obtain MQWs on ZnO such as: ramping up the growth temperature of the barrier, growth interruption, and N_2 or N_2/DMHy annealing after LT-GaN buffer growth. However, these studies did not show significant improvement.

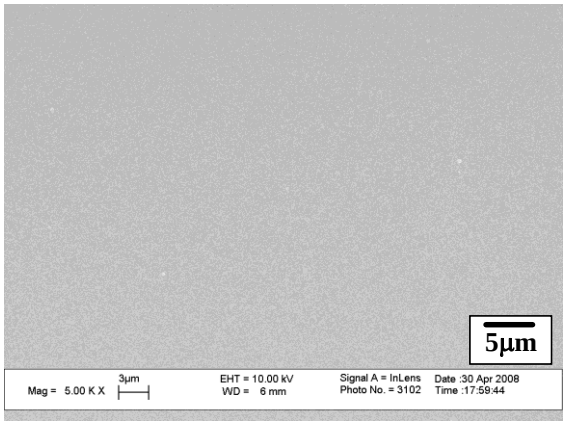


Figure 8: FESEM image of GaN surface grown on 20 nm annealed Al_2O_3/ZnO substrates.

After the optimization, the MQW recipe with a HT-GaN buffer layer was grown on 20 and 50nm ALD-Al_2O_3/ZnO substrates. The 1st

order peak of the satellite peaks for MQWs showed up on the 20nm sample, Figure 6. This peak is much stronger than on the bare ZnO substrate grown before. However, there are no significant satellite peaks to be found for the 50nm case. It is believed the 20nm ALD-Al_2O_3 after 5 minutes annealing can provide the proper nucleation surface for subsequent growth, and good quality MQWs can be effectively grown on ALD-Al_2O_3/ZnO substrate. These results were consistent with calibration runs on bare ZnO where no peaks showed up in the 50nm ALD layers but did show for the 20nm layers.

The $2\theta/\omega$ HRXRD scan for the epitaxial GaN layers grown at 800ºC on 20 and 50nm Al_2O_3/ZnO substrates with 10 and 20 minutes annealing are shown in Figure 7(a). The peaks with the higher intensity are the diffraction from the ZnO (0002) plane of ZnO bulk materials. Moreover, a second peak can only be seen on the 20nm sample. This result shows that the (0002) plane of the wurtzite GaN was successfully grown on the 20nm Al_2O_3/ZnO substrate. However, the growth of a GaN layer is not realized on the 50nm Al_2O_3/ZnO substrate. It is possible that the thicker Al_2O_3 film has a weaker structural relationship with the underlying ZnO substrate after crystallization. Therefore, the polycrystalline 20nm α-Al_2O_3 may possess highly textured orientation with hexagonal ZnO compared to 50nm samples to assist the nucleation of the GaN layer at the initial stage. In addition, FE-SEM shows a mirror-like GaN surface with no observation of etched pits or peeling off from the 20 nm sample, Figure 8.

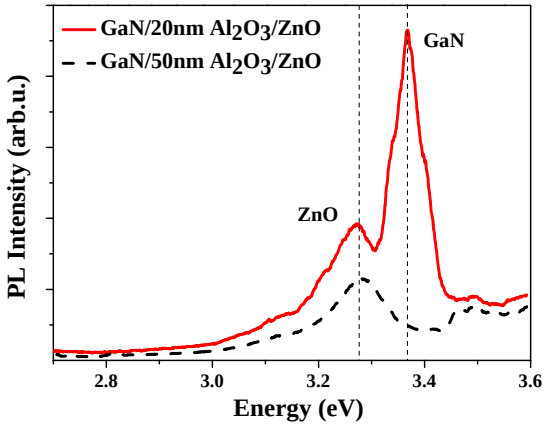


Figure 9: RT-PL spectra of GaN layers grown at 850ºC on 20 and 50 nm annealed Al_2O_3/ZnO substrates by MOCVD.

RT-PL was performed with a HeCd laser of a 325 nm monochromatic beam for the GaN layers grown at 800ºC on 20 and 50nm Al_2O_3/ZnO substrates, Figure 7(b). The ZnO substrate emission can be seen at 3.28eV, which is consistent with the emission seen for bare ZnO substrate. Only a shoulder appeared at 3.39eV in the 20nm sample which is attributed to the near-edge emission of GaN. This emission is a 30meV red-shift from the typical band-edge emission of GaN at 3.42eV. Moreover, a significant near-edge emission of GaN for an 850ºC growth on a 20 nm sample is found to be around 3.36 eV; whereas, the 50 nm sample does not show any GaN peak, Figure 9. This 20 nm sample still shows a red-shift of 60 meV. It was reported that the zinc doping into the GaN or zinc diffusion into the InGaN from the ZnO substrate forms a deep level inducing a red-shift emission of ~0.4~0.5 eV [5-7]. It has been reported that the oxygen substitution for nitrogen acts as a shallow donor in unintentionally

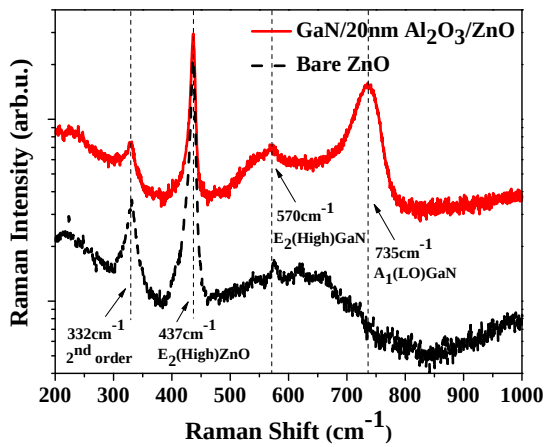


Figure 10: Raman spectroscopy of GaN/20 nm Al_2O_3/ZnO structure and bare ZnO substrate.

doped GaN [8]. It is possible that the oxygen in the GaN layers is from the crystallized Al_2O_3 film where oxygen diffuses out. As a result, the oxygen diffusion into the GaN could form an oxygen-related level as a shallow donor below the conduction band that induces the red-shift. Therefore, these slight red-shifts may be caused by oxygen contamination in the GaN layers instead of zinc. In addition, the various oxygen concentrations in GaN might alter the shifting energy of the two samples due to growth at different temperatures.

It has been reported that Raman scattering is a straightforward method for distinguishing wurtzite GaN [9]. Here, Raman spectroscopy has been carried out on a bare ZnO substrate and a GaN layer grown at 800ºC on 20nm Al_2O_3/ZnO substrate to confirm the HRXRD and PL results, Figure 10. These studies were recorded at room temperature in back scattering Z(x,x)$\underline{Z}$ geometry, with the Z-direction along the c-axis using a laser with λ_{exc} = 488nm. The prominent characteristics of the bare ZnO substrate are observed at 437cm^{-1}, which corresponds to the E_2(high) mode, and at 332cm^{-1}, which correspond to a 2-phonon line. Moreover, the E_2(high) and A_1(LO) modes of GaN phonon peaks were clearly identified in the spectra at 569 and 735cm^{-1}, respectively. These results indicate the presence of a well-crystallized wurtzite GaN layer on 20nm Al_2O_3/ZnO substrates.

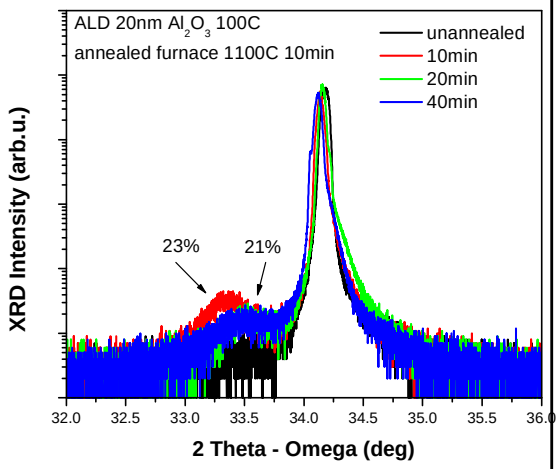


Figure 11: HR-XRD 2θ-ω scans of InGaN layers grown on annealed 20nm Al_2O_3/ZnO substrates.

3.1.3 Epitaxial growth of $In_xGa_{1-x}N$ layers on Al_2O_3/ZnO substrates

InGaN was grown on 20nm Al_2O_3/ZnO and showed that InGaN layers can be successfully grown on Al_2O_3 deposited ZnO substrate after crystallization. The 2θ/w HRXRD scan shows two well-separated peaks from the ZnO substrate and InGaN layers, as seen in Figure 11. InGaN (0002) diffraction peaks were obtained on 20nm Al_2O_3/ZnO substrates, which were annealed at 1100ºC at various times of 0, 10, 20, and 40 minutes. It was seen that the intensity of the InGaN peaks decreased with increasing annealing time. The annealing time of Al_2O_3/ZnO substrates was found to affect the quality of the InGaN layer. Moreover, no InGaN (0002) peak was seen on the un-annealed sample. This observation is highly correlated to the annealing time of 10 minutes for the 20nm Al_2O_3 films, which possessed the highest crystallization. Shifts seen in the InGaN peaks denote different indium incorporation. This could be due to the different surfaces being grown on, which will change the nucleation density as well as the growth mode of the

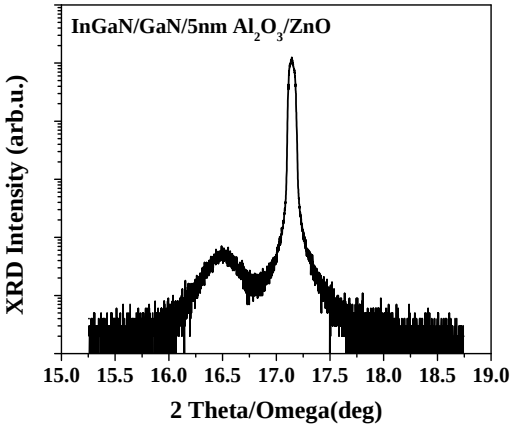


Figure 12: HRXRD 2θ/ω scan of InGaN layers grown on annealed 5nm Al_2O_3/ZnO ZnO substrates.

subsequent GaN and InGaN epilayer. Therefore, the indium composition can be changed due to surface differences.

Following the InGaN growth on furnace annealed 20nm Al_2O_3/ZnO, *in-situ* annealing was attempted as a means to anneal and grow in only one apparatus. Thin ALD layers were grown first to begin the study. Therefore, *in-situ* annealing of a 5nm Al_2O_3/ZnO substrate at 900^{o}C for 20 minutes in N_2 ambient was attempted in the MOCVD chamber right before growth of the InGaN layer. HRXRD measured a successful growth of a single phase InGaN on 5nm annealed Al_2O_3/ZnO, as can be seen in Figure 12. The concentration of indium from the InGaN layer was calculated by the shift of the (0002) InGaN peak position relative to the (0002) ZnO peak position via Vagard's law. An indium concentration of 32% was calculated for this sample. OT measurements were also performed on an InGaN layer grown on bare ZnO to compare with the 5nm Al_2O_3/ZnO sample. Two obvious steps appeared in each curve, corresponding to the absorption edge of ZnO and InGaN. Both spectra exhibit a sharp and transmission wavelength edge at 387nm, which was attributed to the underlying ZnO substrates. The InGaN optical absorption edge can be determined by the sigmoidal fitting seen in Equation 2 [10,11]:

$$T(E) = \frac{T_0}{1 + \exp(\frac{E_g - E}{\Delta E})} \quad (2)$$

where T is the transmission, Eg is the bandgap of the alloy, and ΔE is the broadening parameter, which is equivalent to the Urbach tailing energy. Both of the bandgaps for InGaN grown on bare ZnO and on annealed Al_2O_3/ZnO substrates were calculated to be about 2.43 and 2.51eV, respectively. It is indicated that the bandgap energy of InGaN was not altered significantly when grown on annealed Al_2O_3/ZnO substrates. Taking the bandgap of InGaN on 5nm Al_2O_3/ZnO and putting it into the following equation: E_g(strained) = 3.42 – 0.65x – 3.4159x(1-x) where E_g = 2.43eV gives 34% indium concentration, which is close to the HR-XRD measurement [12].

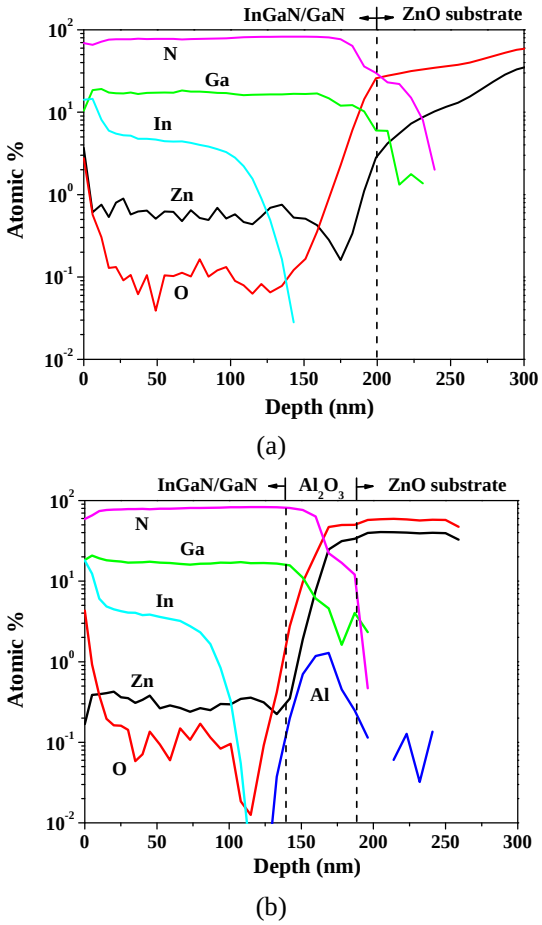


Figure 13: AES atomic depth profile of InGaN layers grown on (a) bare ZnO and (b) annealed 5nm Al_2O_3/ZnO substrate.

The atomic depth profiles of InGaN layers grown on bare ZnO and 5nm annealed Al_2O_3/ZnO substrates are shown in Figure 13(a) and (b). The diffusion of Zn can be clearly observed from the ZnO substrate into the InGaN layer for both cases, as seen in Figure 13(a). The concentration of Zn in the InGaN layer grown on bare ZnO substrate is around 0.7at.%. Moreover, the concentration of Zn is reduced to 0.3at.% when grown on annealed Al_2O_3/ZnO substrate, Figure 13(b). It is noticed that the 5nm Al_2O_3 can

retard the Zn diffusion but the amount of Zn-content still needs to be further reduced. The Zn diffusivity was also evaluated in the case of bare ZnO substrates. The schematic diagram of the InGaN/GaN/ZnO structure can be seen in Figure 14. The Zn atomic flux from the ZnO substrate into the InGaN layer can be calculated by Equation 2 [13]:

$$J_{Zn} = \frac{T \cdot A \cdot \rho \cdot f_{zn} \cdot N_0}{M_{Zn} \cdot t \cdot A} \tag{3}$$

where T is the InGaN thickness; A is the epilayer area; ρ is the density of InGaN with 32%In, 6.3 (g/cm^3); f_{Zn} is the Zn weight fraction in InGaN, 0.01; N_o is Avogadro's number; t represents the growth time, 30min; and M_{Zn} is the atomic weight of Zn. Substitution of all the values above into Equation (4) yields J_{Zn}= 2.75x10^{12} (atom/cm^{2}s). The Zn atomic flux in the GaN buffer layer, J_{Zn}, also can be expressed by Fick's second law assuming the Zn concentration gradient is linear. Therefore, the diffusivity of Zn in the GaN can be obtained by Equation 4 [14]:

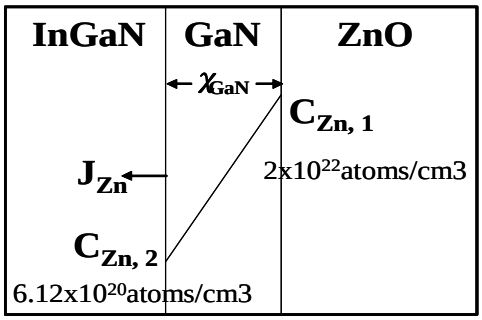


Figure 14: Schematic drawing of the interfaces for Zn atomic flux calculation from the bare ZnO substrate into the InGaN layer.

$$J_{Zn} = D_{Zn} \frac{C_{Zn,2} - C_{Zn,1}}{\chi_{GaN}} \tag{4}$$

where D_{Zn} is the Zn diffusivity in the GaN, χ_{GaN} is the thickness of the GaN layer, $C_{Zn,1}$ is the theoretical Zn concentration in ZnO, (2x10^{22}atoms/cm^3), and $C_{Zn,2}$ is the Zn concentration in InGaN, (6.12x10^{20}atoms/cm^3), which can be obtained from the AES atomic depth profile. Therefore, D_{Zn} is calculated to be about 2.37x10^{-16}cm^2/sec. This diffusivity of Zn in GaN at 700^{o}C is in the same order as the Zn diffusivity in GaN at 930^{o}C (1x10^{-16}) [15]. The concentration of O in the InGaN layer was at a consistent value of 0.1% with and without the Al_2O_3 film deposited. The thicknesses marked in Figure 13 are only observations. Figure 13(a) might have different thicknesses due to etching of the ZnO substrate during growth, which induces the non-uniformed interface of each individual layer. The Al_2O_3 spreading in Figure 13(b) could be caused by post-annealing and diffusion during epilayer growth. Therefore, its thickness during atomic depth profile measuring could seem larger.

Table 9: Summary of ex-situ annealing conditions for ALD-grown Al_2O_3/Si samples.

Thickness (nm)	Temperature (°C)	Time (sec)	Atmosphere
10	1300	90	Air
10	1100	30	N_2
10	1200	30	N_2
10	1200	90	Air
10	1200	180	Air
20	1100	30	N_2
20	1000	120	N_2
20	1100	120	N_2
20	1200	120	N_2
30	1100	30	N_2
30	1200	30	N_2
50	1200	90	Air
50	1200	180	Air

100	**1300**	**90**	**Air**
100	**1200**	**90**	**Air**
100	**1200**	**180**	**Air**
100	**1100**	**90**	**Air**
100	**1100**	**180**	**Air**
100	**1200**	**90**	**Air**

3.2 Year 2

Year 2 work has focused on the MOCVD growth of high-quality GaN thin films and LEDs on Si substrates using an ALD-Al_2O_3 interlayer. Growth processes were developed for both the Al_2O_3 layer and GaN thin films on bare Si. This process was then transferred to ALD-Al_2O_3/Si substrates for growth of GaN-based LEDs on Si. The LEDs were then investigated for efficiency, particularly IQE. LEDs on Si show similar performance to comparable structures on GaN/sapphire templates.

3.2.1 Experimental

All GaN thin films in this study were grown using a modified commercial MOCVD system with a vertical injection, rotating disk configuration. The Al_2O_3 layers were deposited using a custom-built ALD system with trimethyl aluminum (TMAl) and H_2O as Al and O precursors, respectively. Al_2O_3 films ranging in thickness from 2 nm to 200 nm were investigated in this study. GaN thin films were grown by MOCVD on bare ZnO (0001) and Si (111) substrates to provide a baseline process from which to work when growing on Al_2O_3 substrates. ZnO substrates were cleaned with acetone for 3 minutes and methanol for 3 minutes, then rinsed in deionized water and blown dry with N_2. All Si substrates used in this work were cleaned before deposition by dipping in Hydrofluoric acid for 1 minute to remove the native oxide layer and then rinsing in deionized water for 1 minute. GaN layers were grown on both simple AlN buffer layers and buffer structures containing LT-AlN interlayers. The growth process was then transferred to Al_2O_3/Si substrates. The properties of these films were studied to determine the effect of the Al_2O_3 layer on the subsequent GaN layer, and to develop an MOCVD growth process for GaN on sacrificial substrates that can consistently yield device-quality material.

Structural properties of the thin films were investigated using a Philips X'Pert Pro MRD four circle diffractometer and a Renishaw micro-Raman system with a 488 nm Ar-ion laser. A PSIA atomic force microscope (AFM) was used to study surface morphology. Photoluminescence spectra were taken with two different experimental setups. A 325 nm Melles-Griot HeCd laser with an Acton Spectra Pro 2300i monochromator and PIXIS 100 CCD camera was used for temperature-dependent measurements. A 248 nm Ne-Cu laser with a CVI monochromator and a Hamamatsu photomultiplier tube (PMT) was used for room temperature measurements. Electrical properties were studied using a HEM2000 Hall Effect Measurement system from EGK Co., Ltd. The process was then used to grow GaN-based LED structures on both bare Si and Al_2O_3/Si substrates. These devices were investigated for efficiency (specifically, IQE), and the devices on Si showed similar performance to comparable devices on sapphire, showing great promise for Al_2O_3/Si as a substrate technology for MOCVD growth of GaN.

3.2.2 ALD-grown Al_2O_3 layers on Si(111)

Structural properties of the ALD-grown Al_2O_3 layers on Si(111) were studied using XRD. XRD on the as-deposited samples showed no peaks that could be attributed to the Al_2O_3 layer. This suggests that the layers are amorphous, so annealing studies were done to improve crystal quality and provide a more suitable surface on which to nucleate for GaN growth. Ex-situ annealing studies were done using an MHI high temperature tube furnace under either N_2 or air ambient. A summary of the ex-situ annealing conditions that were investigated is shown in Table 9. Al_2O_3 thickness, annealing time, temperature, and atmosphere were varied in this study.

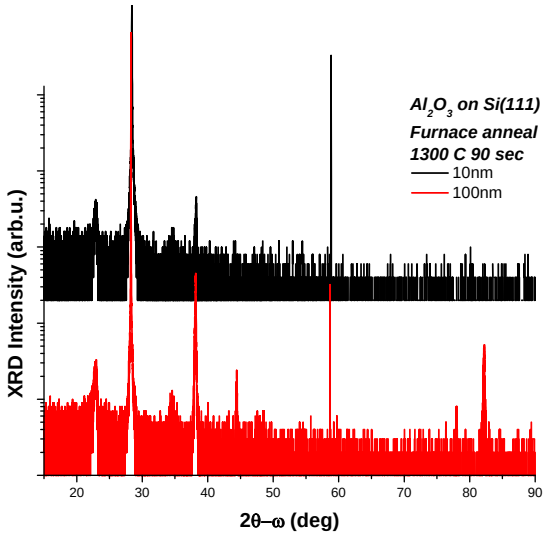


Figure 15: XRD 2θ-ω scans of 10 nm and 100 nm Al_2O_3 layers on Si, both annealed at 1100°C for 90 seconds.

Multiple crystalline phases were observed via XRD upon annealing, though the crystallinity of the Al_2O_3 layers remains low. Five different peaks were observed in the XRD spectra, and the presence and behavior of each one depends on the layer thickness and annealing conditions. Figure 15 shows XRD spectra from two Al_2O_3 layers (10 nm and 100 nm) that were annealed at 1300 °C for 90sec. Peaks near $2\theta = 22°$, $2\theta = 34°$, and $2\theta = 38°$ appear in both samples, and an additional two peaks near $2\theta = 44°$ and $2\theta = 82°$ appear in the 100 nm sample. These last two peaks only appear in the XRD patterns of the thicker (>20 nm) samples, suggesting either increased crystal quality in these samples or formation of multiple phases.

The two most significant peaks are the peak near $2\theta = 34°$, which is attributed to the Al_2O_3 (104) reflection, and the peak near $2\theta = 38°$, which is attributed to the Al_2O_3 (110) reflection. The dependence of the FWHM of these peaks on both thickness and annealing temperature was plotted, and a 3D surface was fit to the data points. Figure 16(a) shows the dependence of the Al_2O_3 (104) peak on thickness and annealing temperature in air, and Figure 16(b) shows the same dependence, annealed in nitrogen. Figure 16(c) and (d) represent the FWHM dependence of the Al_2O_3 (110) peak annealed in air and nitrogen, respectively. The most interesting dependence is the Al_2O_3 (110) peak annealed in air, suggesting that thicker samples annealed at higher temperatures show a higher degree of crystallinity in the (110) reflection. The difference between samples annealed in air and those annealed in nitrogen is most likely to due to the presence of oxygen at the surface when annealing in air. This additional oxygen may allow for the formation of fewer point defects during annealing, leading to higher crystal quality compared to the samples annealed in N_2. However, surface morphology of these samples also changed significantly from both the as-grown layers and the thinner layers annealed at lower temperatures.

SEM images reveal more about the effects of heat treatment on the Al_2O_3 layers. All as-grown layers were quite smooth, with a mirror-like surface, and the thin layers (≤20 nm) showed relatively little change in surface morphology with annealing up to 1300 °C. Significant changes were observed, however, for thicker samples. The 100nm layer shows the formation of circular pits up to ~10 μm in diameter, while the 10 nm layer remains smooth after annealing. These pits were investigated further by energy dispersive spectrometry (EDS) to determine their

composition. EDS measurements were taken on both the smooth surface of the Al_2O_3 film and inside the circular pits. Composition of the samples on both the smooth surface and inside the circular pits is shown in Table 10. The smooth surface is Al_2O_3, while the circular pits are holes in the Al_2O_3 layer that extend all the way to the Si substrate. Though the exact origin of these pits remains unclear, they are clearly more prevalent in the thicker Al_2O_3 layers and most likely have a significant effect on subsequent GaN growth.

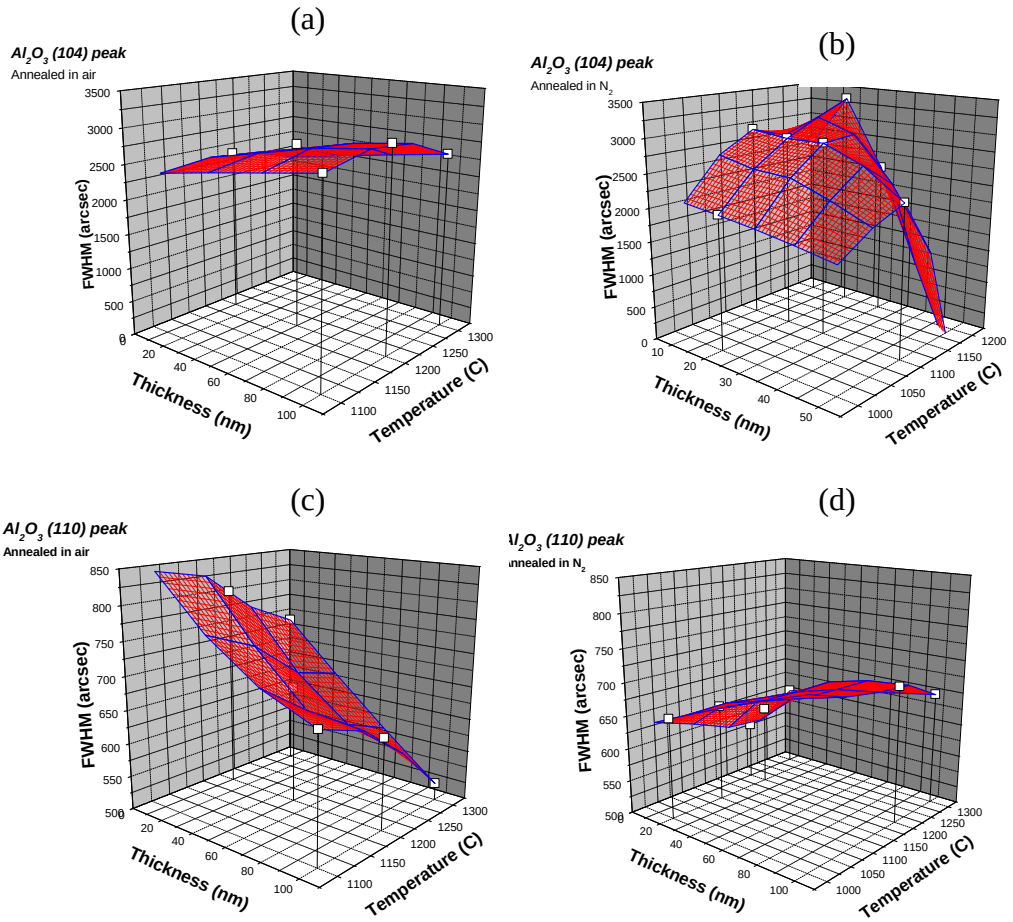


Figure 16: Dependence of XRD FWHM of the Al_2O_3 (104) peak on layer thickness and annealing temperature in air (a), and nitrogen (b). Dependence of XRD FWHM of the Al_2O_3 (110) peak on layer thickness and annealing temperature in air (c), and nitrogen (d). Note the sharp decrease in linewidth for thicker layers annealed at high temperatures in air.

Table 10: EDS results showing composition of the Al_2O_3

Al_2O_3 film	Elements	Wt.%	At.%
Smooth surface	O	47.82	58.85
	Al	49.13	38.29
	Si	3.05	2.86
Hollow structure	O	4.98	8.66
	Al	0.18	0.25
	Si	94.84	91.09

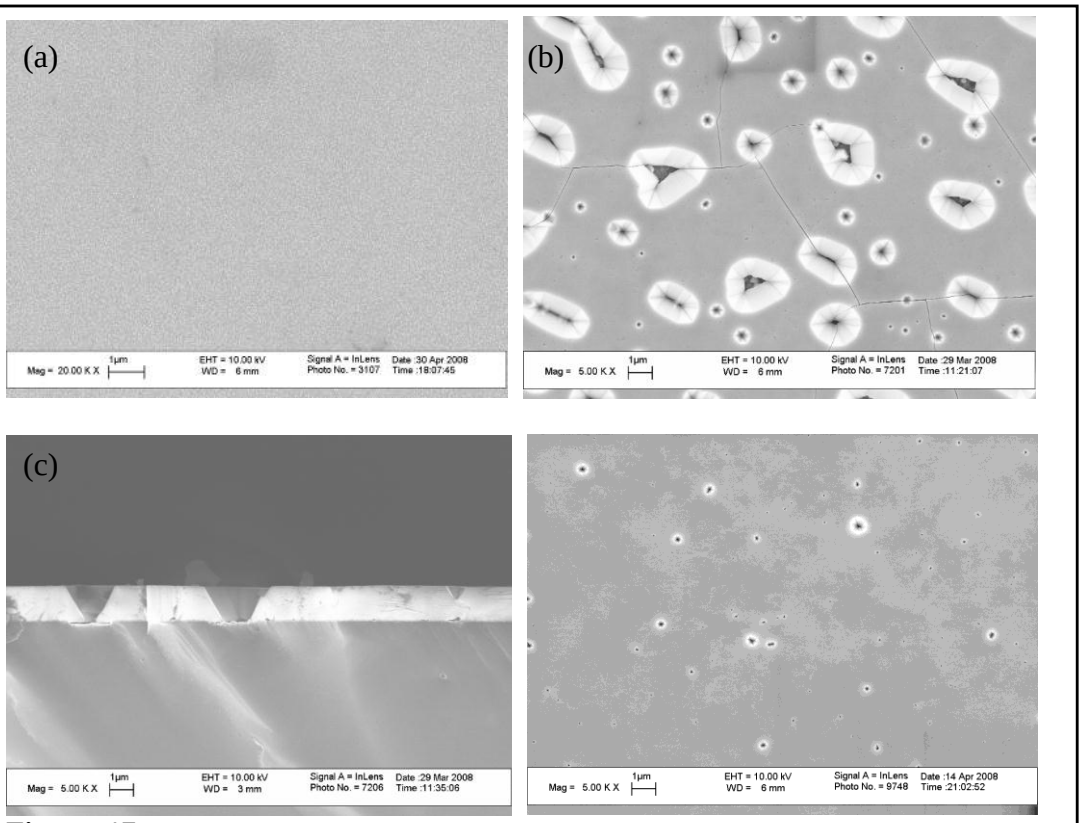


Figure 17: (a) FE-SEM image of the surface of HT-AlN buffer layer grown with V/III ratio=824. (b) Plan-view SEM image of the surface of a GaN layer grown with a LT-GaN interlayer on HT-AlN. (c) Cross-section SEM image showing pits that extend all the way to the substrate. (d) Surface of the sample with a thinner LT-GaN layer, showing fewer and smaller pits.

3.2.3 MOCVD Growth of GaN on bare Si(111)

MOCVD-grown GaN layers were first deposited on bare Si(111) substrates using a high-temperature AlN (HT-AlN) buffer layer to provide a baseline from which to work when growing on the Al_2O_3/Si substrates. The importance of AlN in GaN growth on Si has already been discussed, and the first step toward MOCVD growth in this work was to study the AlN buffer layer quality and to determine favorable growth conditions for this layer. The growth temperature was fixed at ~1060°C, as temperature effects on AlN growth are well-studied. The V/III ratio, however, has a significant effect on AlN quality and is typically much lower than V/III ratios for GaN growth. The V/III ratio in this work was varied from 400 to 1200 to determine favorable conditions for high quality AlN growth. Based on XRD rocking curve scans of the AlN (0002) reflection, a V/III ratio of 824 was chosen for the work moving forward. Figure 17(a) shows an SEM image of the 100 nm HT-AlN layer grown on Si(111) with a V/III ratio of 824. A smooth surface – suitable for GaN growth – is observed at a relatively high magnification of 20Kx.

GaN layers were first grown using the simple AlN buffer layer grown at ~1060°C as described above and a 40 nm-thick low-temperature GaN (LT-GaN) interlayer inserted on the AlN layer in order to relieve strain and increase crystal quality in the GaN layer, similar to GaN growth on sapphire. However, the use of the LT-GaN interlayer led to poor crystal quality as

observed by XRD, with a (0002) rocking curve linewidth of about 1200arcseconds. The linewidth of the near bandedge emission, however, was 37meV, which is near the typical linewidth of ~30meV for GaN on sapphire. Figure 17(b) shows a plan-view image showing pits in the GaN surface. Figure 17(c) shows a cross-sectional SEM image in which these pits extend through the entire thickness of the GaN epilayer. The GaN surface is clearly unable to recover after 1μm of growth, and this may be due to the rough surface of the LT-GaN layer.

A second sample was grown using a thinner (25nm) LT-GaN layer on the AlN buffer layer, and Figure 17(d) shows an SEM image of the surface. It is clear that both the pit density and pit size are significantly reduced, though a few pits remain in the GaN surface. RT-PL also showed an improvement, with a decrease in linewidth to 30meV, though XRD showed no improvement in structural quality compared to the sample with a 45nm LT-GaN layer. Also, both samples using LT-GaN interlayers also exhibited cracking, suggesting that the use of the LT-GaN interlayer does not sufficiently alleviate tensile strain in the material.

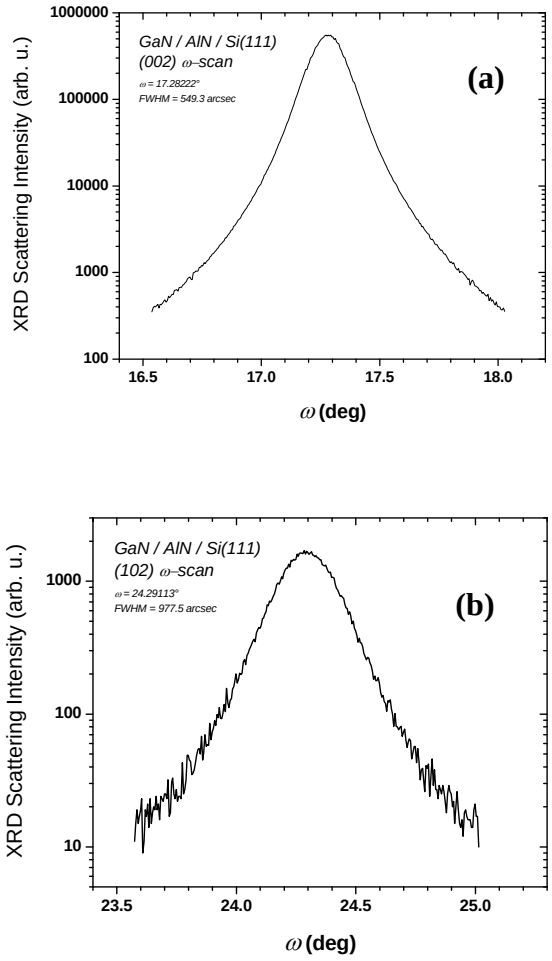


Figure 18: (a) XRD rocking curve scan of the GaN (0002) peak with a linewidth of 549.3 arcsec. (b) XRD rocking curve scan of the GaN (10-12) peak with a linewidth of 977.5 arcsec.

The next step was to remove the LT-GaN interlayer completely and grow a high temperature GaN layer directly on the HT-AlN buffer layer. Removal of the LT-GaN layer resulted in a marked increase in crystal quality. An XRD ω-scan of the (002) reflection is shown in Figure 18(a) for a 1.5μm-thick GaN layer grown at high temperature directly on a HT-AlN buffer layer. Figure 18(b) shows a rocking curve scan of the GaN (102) reflection with a linewidth of 679arcsec, suggesting high crystalline quality GaN layers.

RT-PL spectra of the GaN layers grown with a simple AlN buffer layer show a redshift in the bandedge luminescence, which is most likely due to tensile strain in the layers. Figure 19(a) shows a typical RT-PL spectrum taken from a GaN epilayer on Si. The linewidth of the bandedge emission is 54.8meV. The ratio of bandedge luminescence to yellow luminescence is also relatively low (BL/YL = 5.396) compared to GaN on sapphire, which may be an indication of a higher defect density in the layers on Si.

Figure 19(b) shows an AFM image of the same layer with root mean square (RMS) surface roughness of 5.67Å. While the RMS roughness of these layers is relatively smooth, the sponge-

like surface morphology is an indication that the growth does not proceed in a step-flow like manner. This morphology may also be due to polarity of the films. An Al seeding layer is used in the growth on Si before the AlN nucleation layer, which may in turn lead to N-polar GaN. N-polar material is often reported to show a different (and rougher) surface morphology due to the higher density of dislocations terminating at the surface of the film. Despite the good structural and optical quality of these layers, they remain cracked as a result of tensile strain.

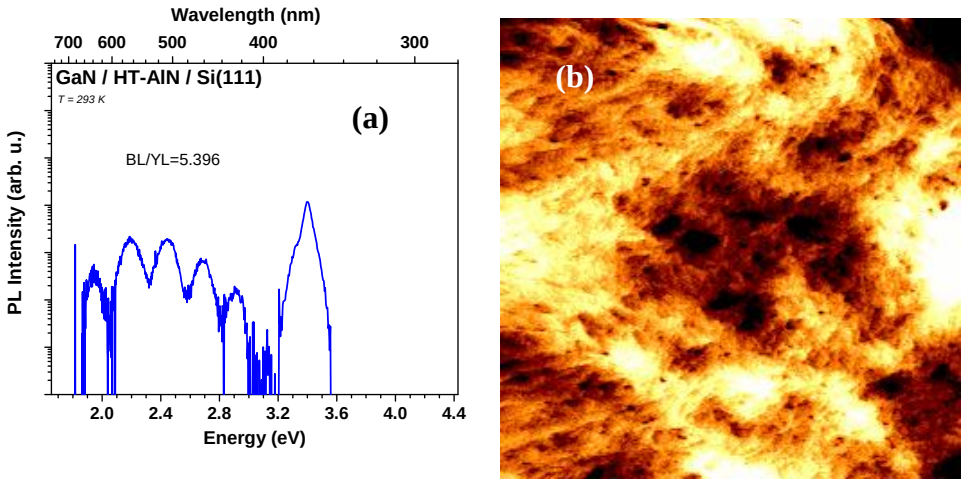


Figure 19: (a) RT-PL spectra (taken with 248 nm Ne-Cu laser) of GaN layer on bare Si with a HT-AlN buffer layer. (b) AFM image of the same layer.

All undoped GaN layers on bare Si exhibit cracks due to tensile strain induced during the process of cooling down. Si, however, is an antisurfactant in GaN growth, and has been shown to relieve strain in GaN on sapphire. Si doping was also studied to determine its effect on strain and relaxation in GaN layers on Si. Figure 20(a) shows a 20x optical microscope image of an undoped GaN layer on Si, while Figure 20(b) shows a 20x optical microscope image of a Si-doped GaN layer on Si. Si doping leads to a significant decrease in crack density of the GaN layers, as seen in the figure. This is due to the fact that Si acts as an anti-surfactant, contributing to strain relaxation in the GaN layer. GaN layers were also grown on Si using LT-AlN interlayers, as has been reported elsewhere [16,17]. A relatively thin LT-AlN layer inserted into the GaN layer helps to relieve strain and increase crystal quality. GaN crystal quality should also

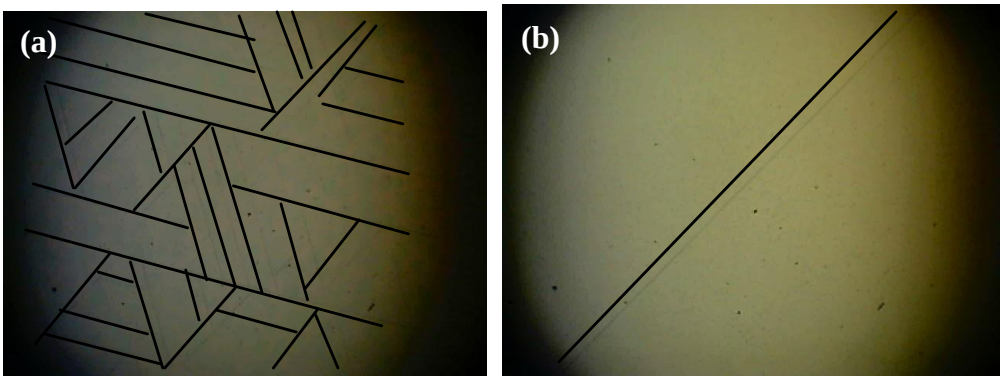


Figure 20: (a) 20x optical microscope image of an undoped GaN layer on bare Si. (b) 20x optical microscope image of a Si-doped GaN layer on bare Si.

increase with an increasing number of LT-AlN interlayers. In this work, three LT-AlN interlayers were used with a thickness of about 20 nm, essentially creating a GaN/AlN superlattice with GaN layers of about 100 nm. The LT-AlN interlayers increased crystal quality compared to the GaN layers grown on Si using a simple AlN buffer layer.

RT-PL measurements were also performed to gain a better understanding of strain and defect formation in the GaN layers. RT-PL spectra clearly show a GaN bandedge with a linewidth of 60.6 meV, though it is redshifted from the unstrained position of 3.42 eV, Figure 21 (a). This redshift is an indication of tensile strain in the epilayers. Figure 21(b) shows a 10 μm x 10 μm AFM image of the surface of this GaN layer. The RMS roughness of the layer is 3.99 Å, and the surface morphology shows more of a step-flow-type pattern than the layers grown with a simple AlN buffer layer. The reason for the change in morphology is not entirely clear. However, it is clear that the use of multiple LT-AlN interlayers reduces the number of dislocations that terminate at the surface of the GaN layer. This change in surface morphology to a more step-flow-like behavior may be related to a reduction in dislocation density in the GaN layers.

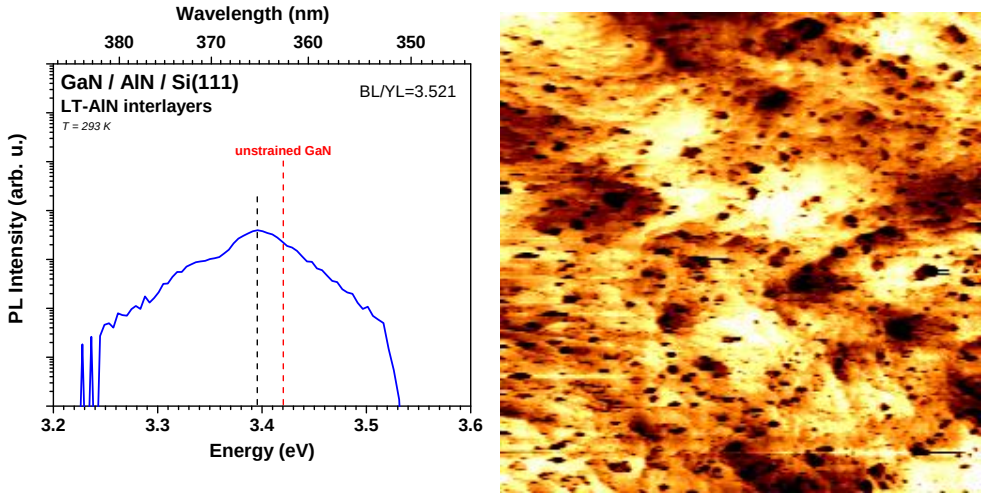


Figure 21: (a) RT-PL spectrum showing the bandedge redshift in GaN layers on Si with LT-AlN interlayers. (b) AFM image of a GaN layer grown on Si using LT-AlN interlayers.

High quality GaN layers on bare Si are very important to gaining an understanding of GaN growth on Al_2O_3/Si. This work has developed an MOCVD process that will consistently yield high quality GaN epilayers on bare Si(111) substrates. High quality GaN thin films, both structurally and optically, have been grown by MOCVD on bare Si substrates. The structural and optical properties of GaN layers grown on bare Si using both a simple AlN buffer layer and LT-AlN interlayers are summarized in Table 11.

Table 11: Summary of GaN properties on bare Si(111)

	XRD		PL		AFM
	(002) FWHM (arcsec)	(102) FHWM (arcsec)	FWHM (meV)	BL/YL	RMS roughness (Å)
HT-AlN buffer	549.3	977.5	49.3	5.396	5.67
LT-AlN interlayers	436.8	1041.9	46.9	5.521	3.99

The major issue, however, remains that the layers are cracked due to tensile strain induced in the epilayer by the thermal mismatch between GaN and Si. ALD-grown Al_2O_3 layers have been introduced to relieve this strain and increase the quality of the subsequent GaN epilayer so that device quality material can be obtained on Si by an MOCVD process. While growth parameters for high quality GaN on Al_2O_3/Si may deviate from those used for GaN on bare Si, the process development done in this section is crucial to gaining a clear understanding of the growth process of GaN on Al_2O_3/Si.

3.2.4 MOCVD Growth of GaN on Al_2O_3/Si

GaN layers were grown on Al_2O_3/Si substrates after the development of a GaN growth process on bare Si. The first step taken in this work was the investigation fundamental growth parameters and structures to lay a foundation for future work. Both LT-GaN and HT-AlN were investigated as buffer layers on the Al_2O_3/Si substrate. GaN growth on sapphire typically proceeds with the growth of a thin (20-30nm) LT-GaN buffer layer before the high quality GaN layer, while growth on Si usually proceeds with a HT-AlN buffer layer ranging from 50nm to 200nm in thickness [18,19]. Both approaches were investigated here, with a HT-GaN layer grown under the same conditions on all buffer layers.

The LT-GaN buffer layers were deposited at 745 ºC with a nominal thickness of 25-30nm, while the HT-AlN buffer layers were deposited at a growth temperature of 1060 °C and thickness of 100nm. Both annealed and unannealed Al_2O_3/Si substrates were used in this study, and the samples grown with the HT-AlN layer consistently yielded higher quality material, as observed by XRD and RT-PL. Table 12 shows results of XRD rocking curve scans on GaN layers grown on both LT-GaN buffer layers and HT-AlN buffer layers on Al_2O_3/Si.

Table 12: Summary of XRD results of GaN layer grown on Al_2O_3/Si with different buffer

Al_2O_3/Si Thickness (nm)	Annealing Conditions	Buffer Layer	GaN (0002) ω-scan FWHM (arcsec)
10	**1100 °C, 90 sec**	**LT-GaN**	**14724**
10	**N/A**	**LT-GaN**	**14724**
10	**1100 °C, 90 sec**	**HT-AlN**	**3672**
10	**N/A**	**HT-AlN**	**4420**

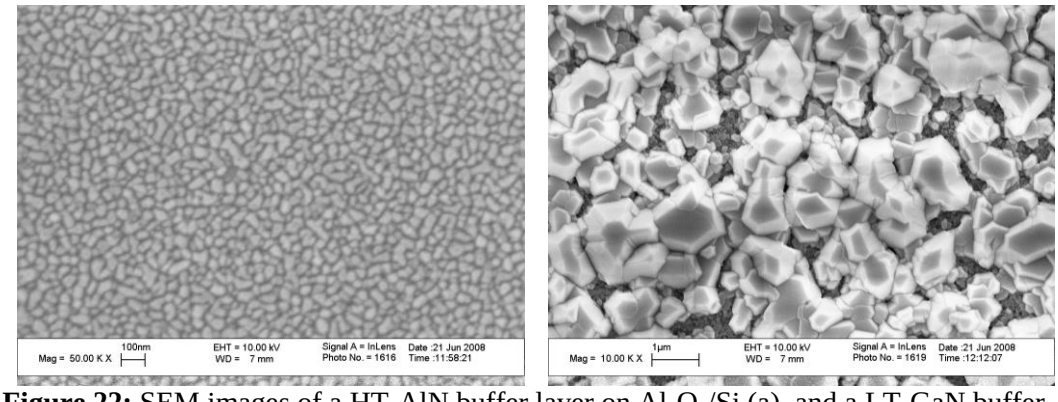


Figure 22: SEM images of a HT-AlN buffer layer on Al_2O_3/Si (a), and a LT-GaN buffer layer on Al_2O_3/Si.

The layer on HT-AlN is much smoother than the layer on LT-GaN. The thickness of the LT-GaN layer is similar to that of LT-GaN buffer layers used on sapphire. However, the polycrystalline nature of the Al_2O_3 film on Si leads to a much rougher surface on the GaN buffer layer. Figure 22 shows SEM images of both a LT-GaN buffer layer and a HT-AlN buffer layer on 10 nm Al_2O_3 annealed at 1100°C for 90 seconds. The HT-AlN buffer layer is much smoother than the LT-GaN layer. This rough surface also affects the growth rate of the GaN layers grown on LT-GaN buffers. The growth rate was significantly slower on LT-GaN buffers than on HT-AlN buffer layers due to surface roughening. This surface roughening decreases mobility of the Ga and N adatoms on the growth surface, leading to a slower growth rate.The growth rate was significantly slower on LT-GaN buffers than on HT-AlN buffer layers due to surface roughening. This surface roughening decreases mobility of the Ga and N adatoms on the growth surface, leading to a slower growth rate.

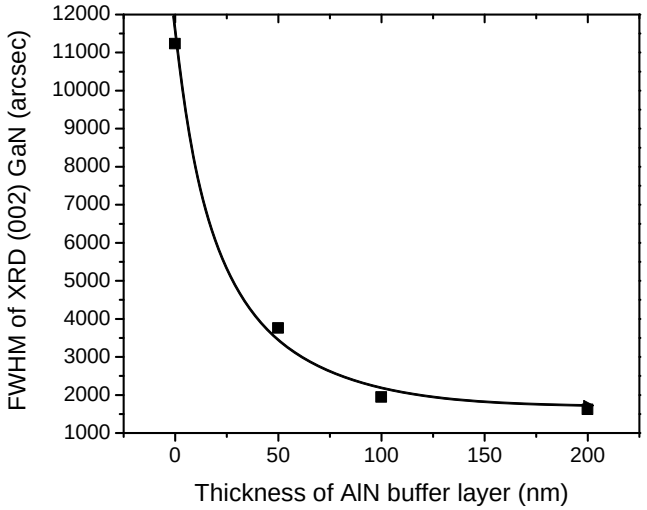


Figure 23: Dependence of the XRD FWHM of the GaN (0002) peak on thickness of the HT-AlN buffer layer.

HT-AlN buffer layers were investigated further because of the smoother surface and higher growth rate of the subsequent GaN layer. The effect of AlN thickness on structural quality of the GaN layer was studied. Figure 23 shows the FWHM of the GaN (0002) ω-scan as it depends on AlN thickness. The structural quality of the topmost GaN layer, as observed by XRD, increased with increasing AlN thickness. However, above a thickness of 100nm, there was only a small decrease in (0002) FWHM. 100nm AlN buffer layers were used in subsequent studies for this reason.

The use of the HT-AlN buffer layers on Al_2O_3, however, introduces another issue that stems from the fact that the AlN layer is grown at a very high temperature (~1060°C). Both the AlN growth temperature and ramp time affect the Al_2O_3 surface prior to growth. The AlN growth temperature is set from previous work, leaving the ramp time as the parameter to be varied. When the temperature ramp time is too short (e.g., 10min.), the Al_2O_3 surface roughens, degrading the surface of the subsequent GaN layer, Figure 24(a). An increase in temperature ramp time to 13 minutes, however, allows for a smoother GaN surface during growth, as can be observed by the clear growth oscillations in Figure 24(b).

Effects of carrier gas on nitride layer growth were also studied using both LT-GaN and HT-AlN buffer layers. H_2 is the most common carrier gas in nitride MOCVD, but many oxide materials, such as ZnO, are not stable in hydrogen. The polycrystalline nature of the Al_2O_3 layers in this study may also allow for H_2 backetching and, thus, decreased crystal quality. N_2 was investigated as a carrier gas for this reason. Growths were performed using both 100% H_2 and 100% N_2 as the carrier gas and LT-GaN as the buffer layer. Figures 24(c) and 24(d) show normal incidence reflectivity data showing the difference between H_2 and N_2 as carrier gases. The surface degrades immediately upon the introduction of TMGa when using H_2 as a carrier gas.

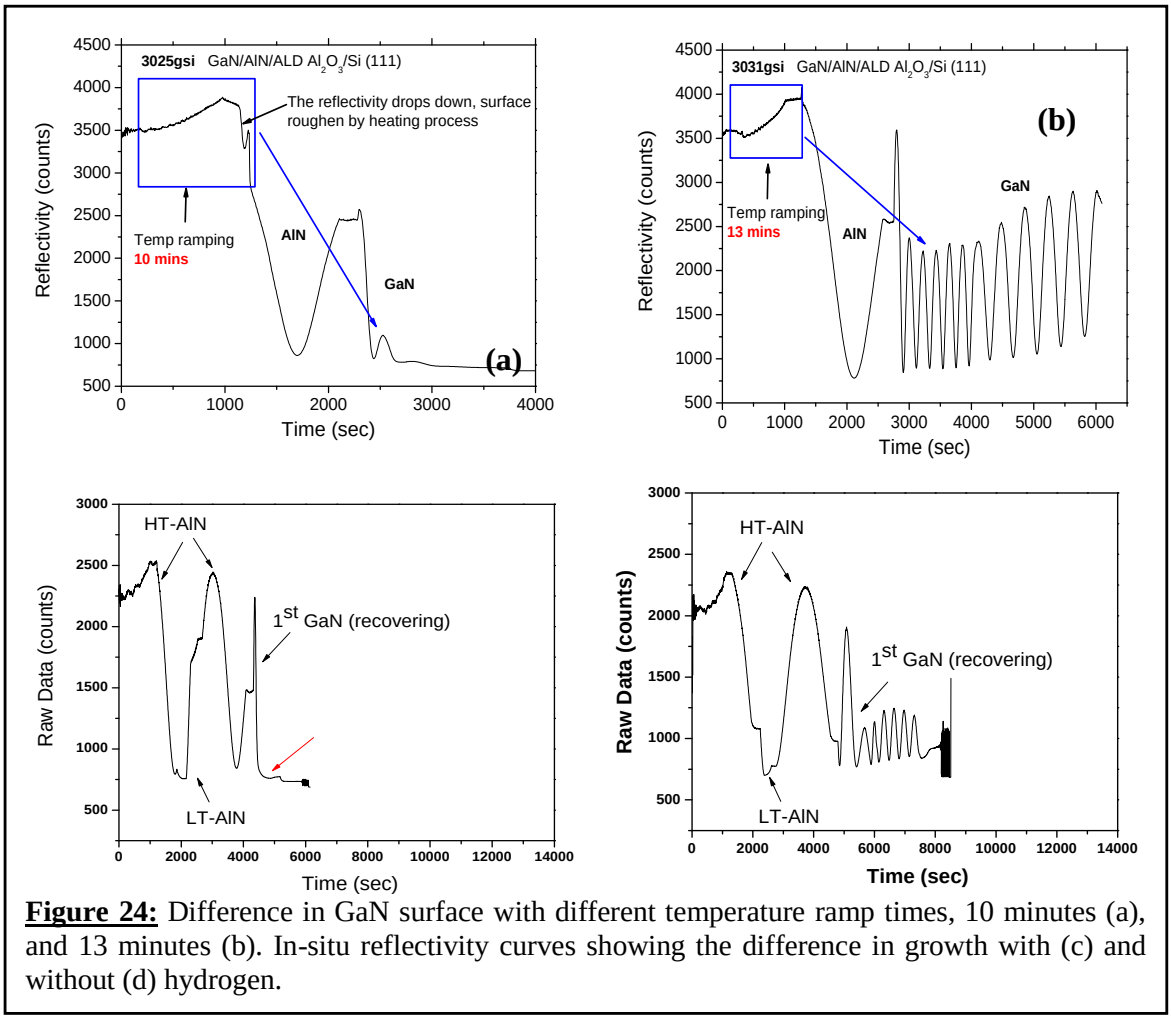


Figure 24: Difference in GaN surface with different temperature ramp times, 10 minutes (a), and 13 minutes (b). In-situ reflectivity curves showing the difference in growth with (c) and without (d) hydrogen.

The use of N_2, however, leads to a smoother GaN surface and clear oscillations due to GaN growth. The degradation of growth surface using H_2 as a carrier gas is most likely due to the etching of the oxide surface during the initial stages of growth, though this is currently unconfirmed.

$Al_xGa_{1-x}N$ layers with different Al composition have also been investigated to grow high quality GaN on Si. Multiple $Al_xGa_{1-x}N$ layers were grown on both bare Si and 10 nm Al_2O_3/Si to act as transition layers for the final GaN layer. Each $Al_xGa_{1-x}N$ layer was 100 nm, with the temperature for each layer being slightly less than the previous layer. XRD results for the samples are shown in Figure 25(a) and (b). Clear $Al_xGa_{1-x}N$-related peaks are observed from the structure on bare Si, one peak from each layer. Peaks from the AlN buffer layer and the topmost GaN layer can also been seen. The structure on 10 nm Al_2O_3/Si also showed the $Al_xGa_{1-x}N$ peaks, though they were much weaker and broader, encompassing all three potential peaks into one. The GaN FWHM on the bare Si structure was 2088 arcsec, while the FWHM on the 10 nm Al_2O_3/Si structure was 5940 arcsec. A second growth was done with only two $Al_xGa_{1-x}N$ layers. The structure for this growth was the previous study except that the third $Al_xGa_{1-x}N$ layer was removed. XRD results, Figures 25(c) and (d), show peaks from both $Al_xGa_{1-x}N$ layers, and these peaks are visible in the structure on bare Si and 10 nm Al_2O_3/Si, respectively.

XRD results show that the material quality improved compared to the growth with three $Al_xGa_{1-x}N$ interlayers. The XRD linewidth of the GaN layer on bare Si was 1944 arcsec, while the FWHM on the 10nm Al_2O_3/Si was 3420 arcsec. These results suggest that $Al_xGa_{1-x}N$/GaN superlattices are not a promising avenue toward improving MOCVD-grown GaN on Si with an Al_2O_3 interlayer, as crystal quality is significantly lower than other work.

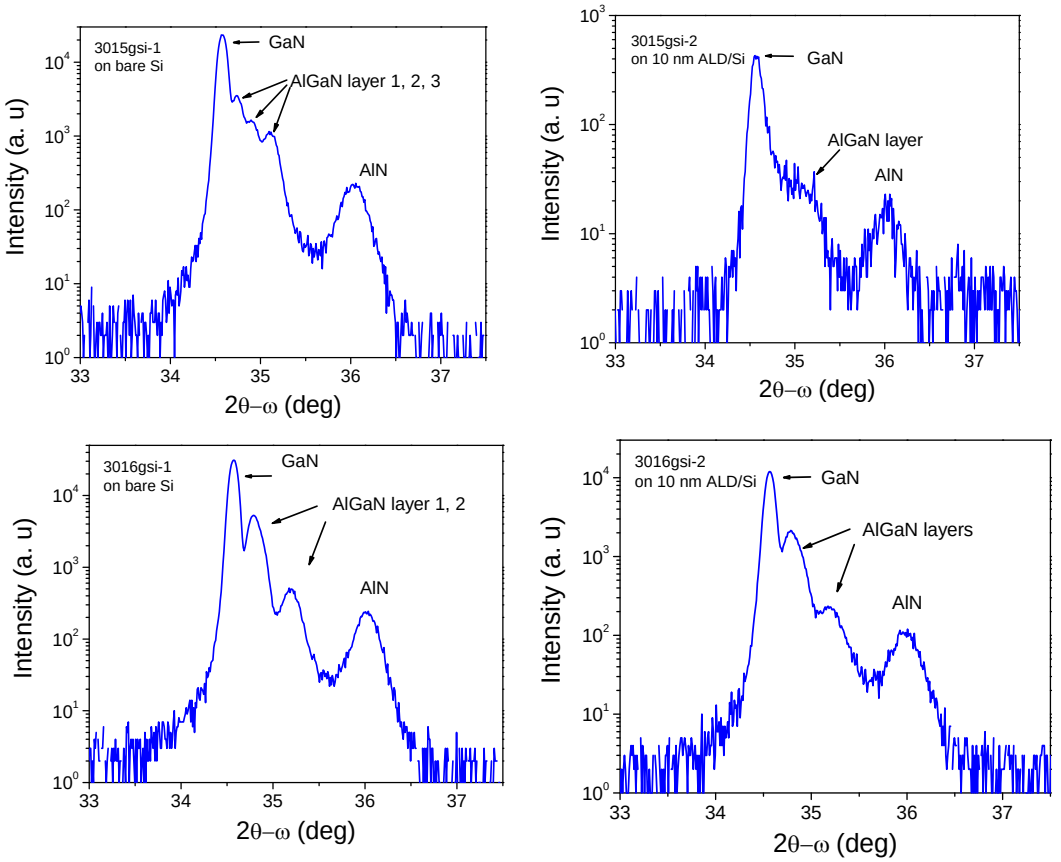


Figure 25: (a) and (b) XRD scans of GaN layers grown on both bare Si and Al_2O_3/Si substrates with three intermediate AlGaN layers. (c) and (d) GaN layers grown on both bare Si (c) and Al_2O_3/Si (d) with two intermediate AlGaN layers.

The effects of the underlying Al_2O_3 layer were studied after initial work was done to determine favorable growth conditions for GaN on Al_2O_3/Si. The effects of Al_2O_3 thickness on the subsequent GaN layer were investigated first. The thickness of the Al_2O_3 layers was varied from 5 nm to 50 nm, and identical GaN layers were grown on each Al_2O_3/Si substrate. Quality for the layers grown on 5 nm and 10 nm Al_2O_3 is similar, but increases somewhat for the sample grown on 20 nm Al_2O_3. After 20 nm, however, the crystal quality of the GaN layer decreases significantly. This is most likely due to the changes in surface morphology that were observed in the ex-situ annealing studies of the Al_2O_3 /Si samples. Thicker Al_2O_3 layers were not studied in further detail for this reason. However, the trends observed for the thinner samples were studied further.

Figure 26 (a) shows a Williamson-Hall plot of a GaN layer on bare Si compared to GaN layers on 5nm, 10nm, and 20nm Al_2O_3/Si substrates. Note the decrease in slope with decreasing

Al_2O_3 thickness. The dislocation density of the GaN epilayers decreases with decreasing Al_2O_3 thickness, but increases significantly when the Al_2O_3 layer is completely removed, Figure 26 (b). The PL bandedge shift was also studied as a function of Al_2O_3 thickness to gain more insight into strain in the layer, and the results are shown in Figure 27(a). The two measurements at zero thickness represent GaN with a simple HT-AlN buffer layer and GaN with three LT-AlN interlayers. The sample with LT-AlN interlayers is blue-shifted from the sample with only a simple HT-AlN buffer layer, indicating a reduction in strain. The Raman E_2(high) mode can also be used as an indication of strain in GaN [20]. Raman spectra in the backscattering configuration

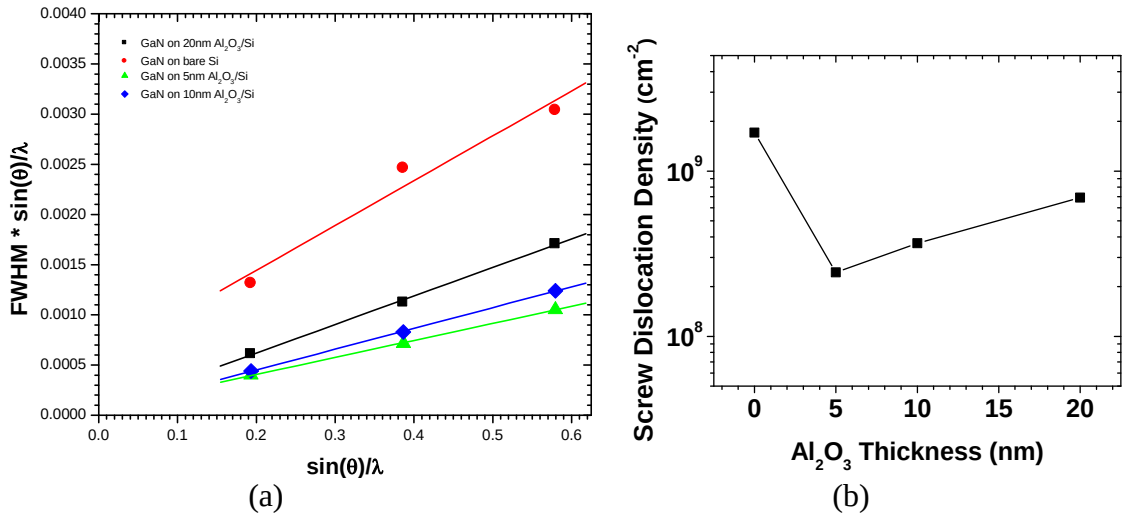


Figure 26: (a) Williamson-Hall plot of the GaN (002) reflection for various oxide thicknesses on silicon. (b) Screw dislocation density of GaN layers on Si(111).

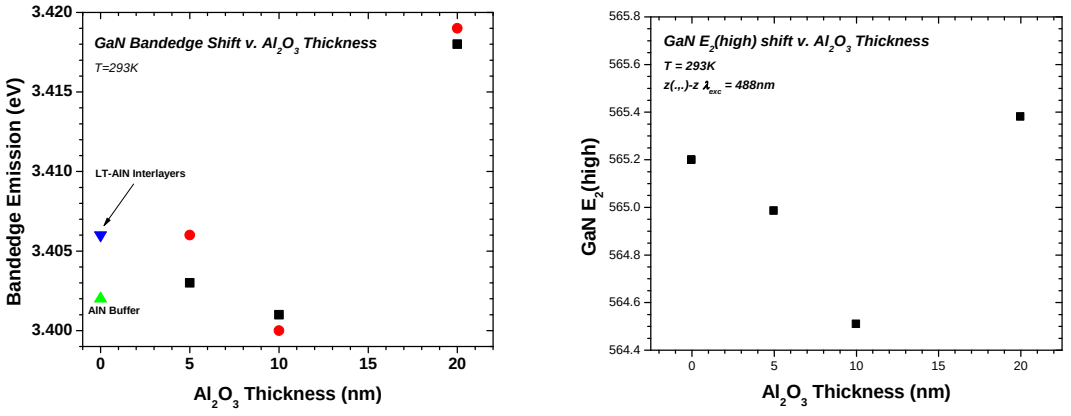


Figure 27: (a) Bandedge redshift with Al_2O_3 thickness. (b) Raman E_2(high) shift with increasing Al_2O_3 thickness due to strain.

were taken, and the shift of the E_2(high) mode was plotted as a function of Al_2O_3 thickness, similar to the bandedge shift, Figure 27(b). These results follow the same pattern as the PL

results. The major point of interest here is the increase in strain when the Al_2O_3 layer thickness increases from 5 nm to 10 nm, and then the reduction in strain with a further increase in Al_2O_3 thickness to 20 nm. While this phenomenon is not completely understood yet, a clear trend is observed in both the Raman data and the PL data suggesting that the Al_2O_3 does in fact help to relieve strain in the GaN layers compared to GaN on bare Si. Table 13 summarizes the properties of the GaN layers grown on both bare Si and Al_2O_3/Si in this work. Material quality improves on the Al_2O_3/Si substrates, and shows great promise toward GaN-based devices on Si.

Table 13: Summary of properties of GaN grown on Si with and without an ALD-grown Al_2O_3 interlayer.

	XRD		PL		AFM
	(002) FWHM (arcsec)	(102) FHWM (arcsec)	FWHM (meV)	BL/YL	RMS roughness (Å)
HT-AlN buffer	**549.3**	**977.5**	**49.3**	**5.396**	**5.67**
LT-AlN interlayers	**436.8**	**1041.9**	**46.9**	**5.521**	**3.99**
5nm Al_2O_3/Si	**378.6**	**849.5**	**46.5**	**7.395**	**3.93**
10nm Al_2O_3/Si	**433.9**	**1344.6**	**47.7**	**4.497**	**5.65**
20nm Al_2O_3/Si	**416.6**	**740.1**	**43.4**	**28.223**	**3.70**

3.2.5 Reduction of dislocation density in GaN on Si

While the FWHM of the XRD rocking curve scans provides a good indication of material quality, a more detailed study was necessary to exactly quantify the material quality and provide a fair comparison to typical GaN epilayers on Si. Figure 26 shows a Williamson-Hall plot based on the GaN (002) reflection, which indicates that the ALD-grown Al_2O_3 leads to a marked improvement in crystal quality, as indicated by the decrease in lineslope. The significant decrease in tilt angle with the introduction of the ALD-Al_2O_3 interlayer is also indicative of a major improvement in crystal quality with the use of the ALD-Al_2O_3 interlayer. Screw dislocation density can also be calculated from Figure 1 using Equation (1):

$$N_{screw} = \frac{\alpha^2}{4.35 \cdot |b_c|^2}$$

where α is the tilt angle and b_c is the burgers vector in the (002) direction. The dislocation densities calculated from Figure 26(a) are shown in Figure 26(b). It is clear that the use of the ALD-Al_2O_3 interlayer reduces the dislocation density in the GaN epilayer by an order of magnitude, from $2x10^9 cm^{-2}$ on bare silicon to $2x10^8 cm^{-2}$ for a 5nm Al_2O_3 layer on Si. This reduction in dislocation density to a level similar to that of GaN on sapphire is a major reason that the GaN-based LEDs grown on ALD-Al_2O_3/Si substrates show similar IQE values.

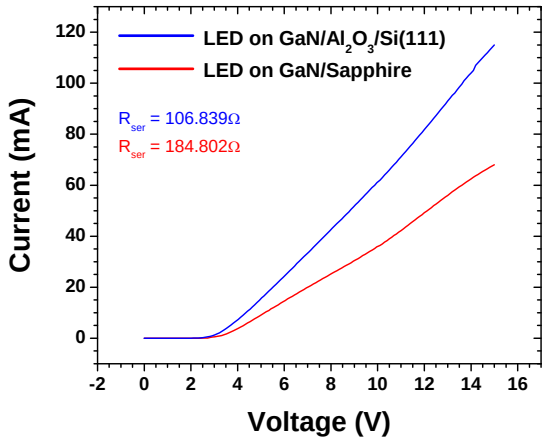


Figure 28: I-V curves for GaN LEDs on both sapphire and Si(111).

3.2.6 Fabrication and Testing of GaN-based LEDs on Si

GaN-based LEDs were grown on both sapphire and Si substrates using the MOCVD growth process developed in previous sections. These devices consisted 1.0 μm of n-type GaN, a four-period $In_xGa_{1-x}N$/GaN MQW structure as the active region, and ~160nm of p-type GaN on top. LEDs were grown on 1.5μm-thick GaN/sapphire templates and on 1.5μm-thick GaN/Al_2O_3/Si templates simultaneously so that similar devices could be obtained on both sapphire and Si. Devices on both Si and sapphire showed a relatively high series resistance, Figure 28, which is most likely related to the p-type contact and current spreading layer. Further optimization of the LED growth process, p-type layer, and p-type contact resistance will result in much higher efficiency of the GaN emitters on both Si and sapphire substrates. However, this work shows that for similar devices on Si and sapphire, the device on Si shows a much lower series resistance. The reason for this decreased series resistance remains unclear, however. Another significant point that is observable from a comparison of the I-V curves in Figure 29 is the turn-on voltage. The turn-on voltage for the device on Si is slightly lower than that of the device on sapphire (~2.9V on Si compared to ~3.0V on sapphire).

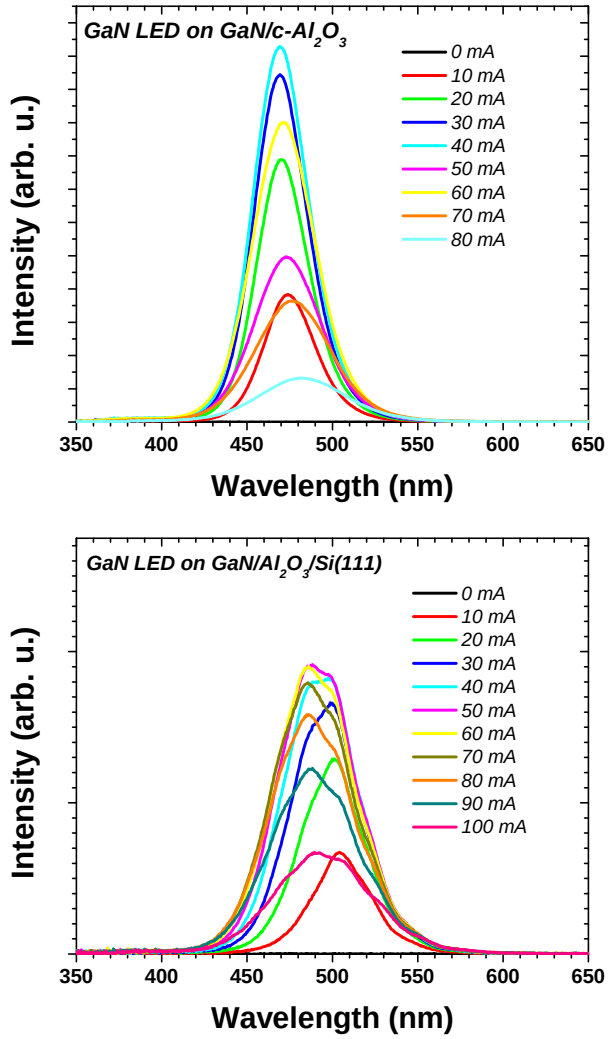


Figure 29: (a) EL of a GaN LED on sapphire with peak emission wavelength near 470 nm. (b) EL of a GaN LED on Si with peak emission wavelength near 490 nm.

Electroluminescence (EL) of the devices was measured at drive currents up to 100mA. EL of a typical device on sapphire is shown in Figure 29(a). The luminescence intensity of these devices reached a peak with a drive current of 40mA. A typical EL spectrum for an LED on Si is shown in Figure 29(b).

The devices on Si show a redshift in peak emission wavelength compared to those on sapphire. This may be due to the higher thermal conductivity of Si compared to sapphire (k_{Si} = 1.3 W $cm^{-1}{}^{\circ}C^{-1}$; $k_{Sapphire}$ = 0.35 W $cm^{-1}{}^{\circ}C^{-1}$). The higher thermal conductivity of Si results in a slightly lower surface temperature compared to the sapphire, which leads to a higher indium content in the layers on Si. The tensile strain induced by the Si substrate may also contribute to higher indium content. This higher indium content in turn leads to longer peak emission wavelength compared to the devices on sapphire.

A shift in peak emission wavelength is also observed with an increase in drive current for both devices. This shift is more clearly seen in the devices on Si, and it may be due non-uniformity of the quantum wells caused by the much higher indium content in the active region of these devices. Luminescence was also measured as a function of drive current for these devices, and results are shown in Figure 30. The comparison is significant because it shows that for comparable devices, the LED on Si shows a much higher efficiency at high drive currents than the LED on sapphire, despite the longer wavelength emission from the device on Si, which often leads to a drop in efficiency.

The IQE of these structures was measured using LT-PL. This approach assumes an IQE of 100% at 8K, and the IQE at room temperature (RT) is calculated as the ratio of PL integrated intensity at RT to PL integrated intensity at 8K. The IQE values for two LEDs that were grown at the the same time – one on sapphire and one on Al_2O_3/Si – are shown in Figure 31(a). As mentioned previously, the device on Si showed a significant redshift in peak wavelength relative to the device on sapphire. However, this redshift did not significantly degrade the IQE, as would be expected with a shift in wavelength from the blue region toward the green region.

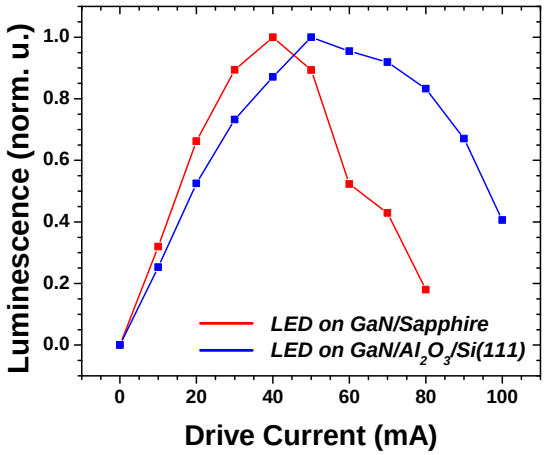


Figure 30: L-I curve for GaN-based LEDs on both sapphire and Si substrates.

Subsequent multiple quantum well structures were grown on Al_2O_3/Si substrates with peak wavelengths shifted further toward the green region. The IQE of these structures was also measured, and a notable drop in IQE was observed with the shift toward longer wavelengths, Figure 31(b).

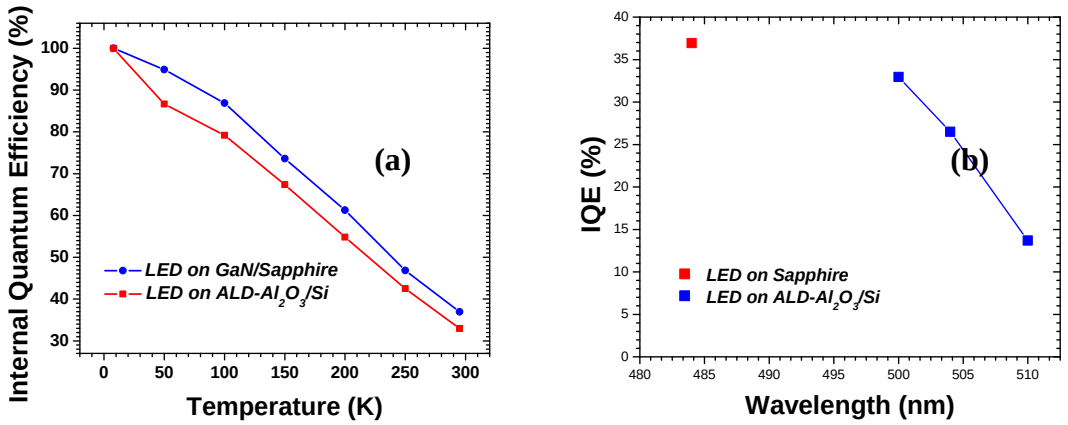


Figure 31: (a) IQE data for GaN LEDs grown at the same time on a sapphire substrate and an Al_2O_3/Si substrate. (b) IQE values for MQW structures on sapphire and Si as a function of peak emission wavelength.

3.3 Year 3

Further optimization was performed and the optimal growth conditions of ALD-Al_2O_3 interlayer, AlN buffer layer, and InGaN/GaN multiple quantum wells active region were implied in the growth of next series of LED structures. Figure 32 (a) shows a 20x optical microscope image of a LED structure on ALD/Si. Majority of the film was crack-free. However, some areas did have cracks with crack separation of roughly a few millimeters. The use of ALD layers with interlayer's can fully eliminate the cracks while maintaining the higher crystal quality of the GaN layer, compared to films grown on bare Si. The schematic of a fabricated LED device is shown in Figure 33 (b). These devices were 350 × 350 μm^2 and consisted of 1.0 µm of n-type GaN, a three-period InGaN/GaN MQWs as active region and 150 nm of p-type GaN on top of the chosen GaN/AlN/ALD/Si templates. The top view of devices under standard LED fabrication processes can be seen in Figure 32 (b,c).

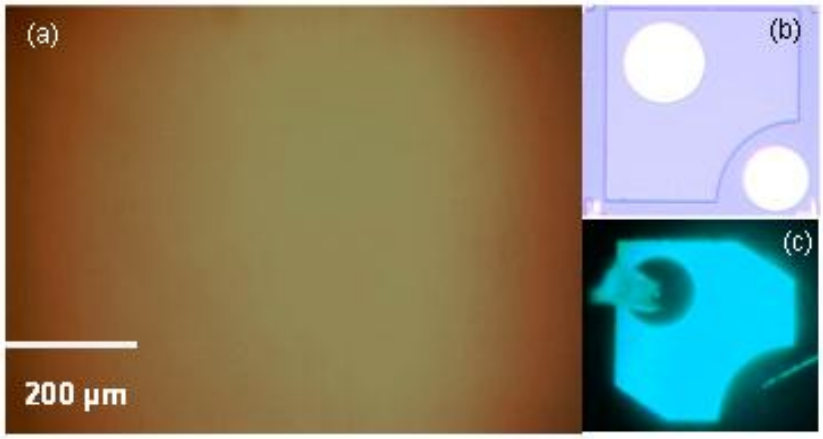
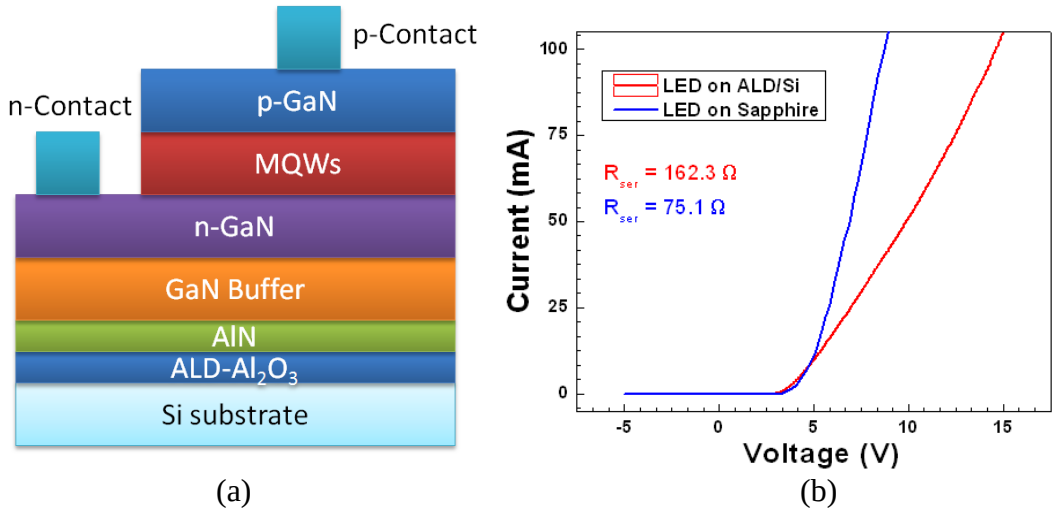


Figure 32: (a) Optical Microscope image of LED film, (b) Top view of fabricatd of LED device, and (c) LED on ALD/Si lighted under normal operating condition.

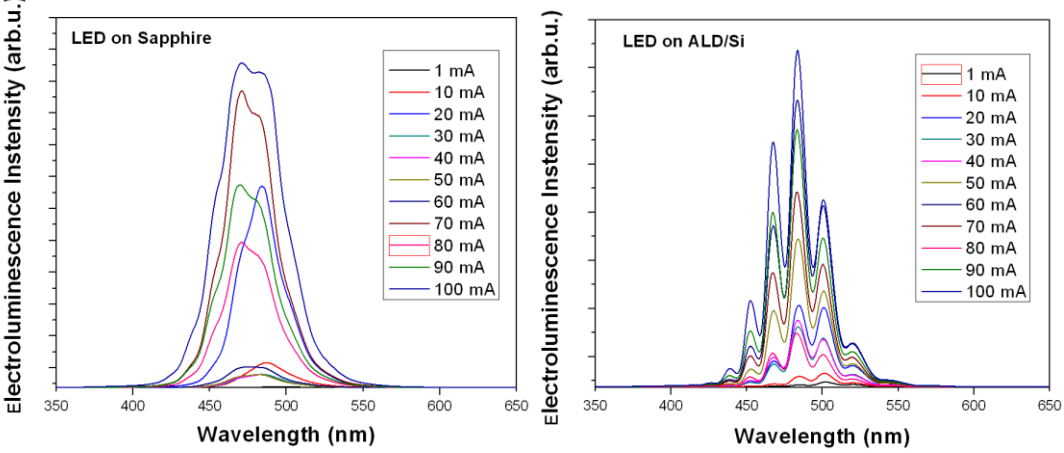


(a) (b)

Figure 33: Illustration of (a) LED structure grown on GaN/AlN/ALD-Al_2O_3/Si after fabrication, (b) I-V measurement of LED devices.

A

nickel oxide current spreading layer was used to ensure uniform current spreading distribution through the device. The uniform light emission from the device surface, as shown in Figure 32(b), indicates good current spreading of the device structure. Electrical measurements were taken using a Keithley 2420 sourcemeter on LED grown on ALD/Si template and sapphire substrate, respectively. The turn-on voltages of two LEDs (~3.0 V) are comparable, as shown in Figure 34 (b). The LED on ALD/Si showed up to 72% reduction in series resistance compared to previous LED devices, although series resistance of both were still higher than LEDs on sapphire. These electrical measurement results clearly indicate substantial improvement in electrical property of our latest LED devices on ALD/Si. However optimization of p-GaN layer, p-contact, and etch depth are still required to further reduce the higher series resistance measured for the devices both on sapphire and Si.



(a) (b)

Figure 34: EL spectrum of (a) LED on sapphire and (b) LED on ALD/Si.

EL spectra of the devices were measured at drive currents up to 100 mA by OL-770 spectroradiometer from Optronic Laboratories. EL spectra as a function of drive current of a LED device on sapphire and on ALD/Si are shown in Figure 34 (a) and (b), respectively. The presence of Fabry–Pérot interference fringes is a characteristic feature for the LEDs grown on Si in Ferguson's lab, which indicated good interfacial quality of the epilayers grown on ALD/Si. From the plot of peak emission wavelength in Figure 35, a significant blue-shift was observed in all LEDs on sapphire with the increase of drive current. However, the blue-shift in LEDs on ALD/Si (~3 nm) is much less compared to that in LEDs on sapphire (~20 nm). The current-induced blue shift,

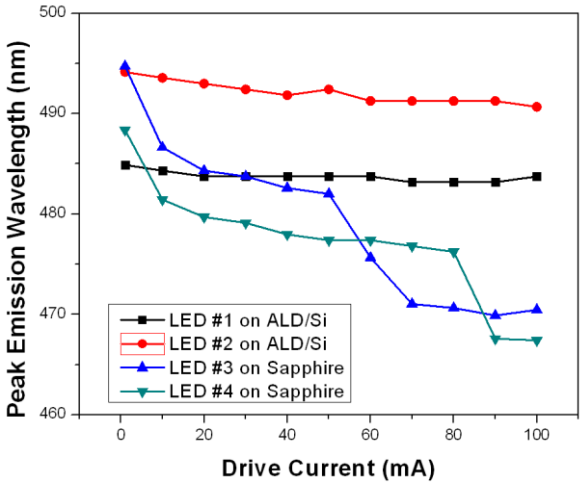
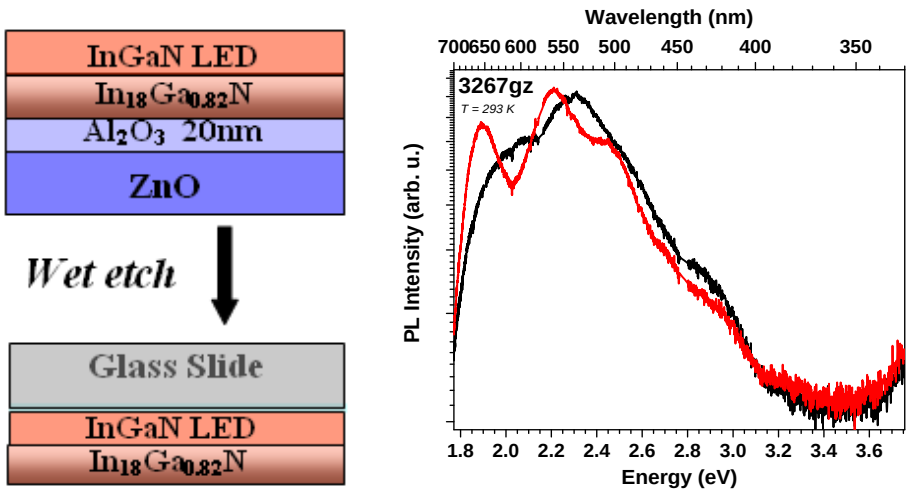


Figure 35: Blue-shift of peak emission wavelength in LEDs on ALD/Si and sapphire. #1 & #2 represent LEDs at different locations on same wafer.

accompanied by a significant spectrum broadening, occurs mainly due to band filling of localized states originating from compositional fluctuation of InGaN alloys. This implies devices on ALD/Si may have comparatively less compositional fluctuation and have stable emission wavelength regarding different drive currents, which is very important to the general lighting system to meet designated requirement of light.

3.3.1 GaN LED on ZnO substrate and substrate removal process

The LED structures consisted of a p-$In_xGa_{1-x}N$ layer on 5 multiple quantum wells (MQWs) on an n-$In_xGa_{1-x}N$ layer were also grown on ZnO substrate. InGaN layers with 18% indium was used as 18% indium allows for InGaN layers to be perfectly lattice matched to ZnO substrates. The use of InGaN layers also allows for lower growth temperatures, which is ideal for growth on ZnO substrates, lowering Zn/O diffusion from the substrate into the epilayers. After growth, the substrate was chemically etched off via HCl etching (10% HCl for 20 minutes) and bonded to a glass substrate. The structure showed emission as seen by the eye and by PL. PL showed InGaN peaks in the 550nm range, as seen in Figure 36. However, no I-V curve was seen, probably because the transport properties were degraded by diffusion of Zn from the substrate into the epilayers during MOCVD growth. Low temperature (LT)-PL was performed to measure the IQE of QWs in this structure. IQE was measured to be about 60%, which was an excellent result and was possibly due to reduced strain in the InGaN quantum wells on ZnO substrates. Etching of the ZnO substrate also showed that removal of the ZnO substrate can be performed easily and the process is much less complicated than the removal of Si from GaN epilayers. However, ZnO poses other challenges, that is, the vulnerability of ZnO substrate in MOCVD environment such as its decomposition in NH_3 ambient and Zn diffusion into GaN epilayers. These growth challenges would need further investigation in the future.



(a) (b)

Figure 36: PL of $In_{0.18}Ga_{0.82}N$ LED on ZnO substrate. The two measurements are from two different spots on the sample.

3. 3. 2 Development of free-standing LED devices on Silicon substrate by wet etching

GaN LED devices on (111) Si substrates were successfully fabricated using ALD-grown Al_2O_3 interlayers developed in previous studies. In order to improve light extraction, it is necessary to remove the silicon substrate. Removing the substrate will eliminate light absorption by Si, while inserting AlN/AlGaN distributed Bragg reflector between template layers and LED structures will introduce more tensile stress into the epilayers in LED structure. This should also improve the forward series resistance in vertical or flip-chip conduction by getting rid of the insulated Al_2O_3 interlayer and the large band offset between Si and upper epilayers.

3.3.2.1 Wet & dry etching

Compared with dry etching using an ICP process, wet chemical etching is a highly established basic processing method in the semiconductor industry for Si. It is a well-controlled, readily accessible, and cheap processing method that is suitable to be employed to remove the silicon substrate in this research. It is therefore expected that through the wet etching process less stress or damage will be caused to the thin LED epilayers with a total thickness of ~3 microns.

3.3.2.2 Deposition of reflection coating

In order to facilitate bonding to the copper substrate, metal reflector and contact layers were deposited on the GaN surface by electron-beam evaporation. Two metal stack configurations were tested, which had the following compositions:

1) 10 nm Ti / 50 nm Al / 50 nm Au / 500 nm In
2) 10 nm Ti / 50 nm Al / 100 nm Cr

Both Au and Cr were identified as widely available corrosion-resistant metals that could be compatible with the Si wet-etch process, and in the first configuration the 500 nm indium layer was used in an attempt to enhance bonding to the metal substrate. Ti was used as an adhesion layer; for LED device structures this layer was replaced by the oxidized Ni/Au Ohmic contact layer.

3.3.2.3 Substrate removal by wet etching

Free-standing LED devices were achieved using selective area wet etching to pave the way for the removal of the entire sacrificial Si substrate. One of the key challenges we encountered is the generation of cracks and occasional warping of the epilayer if the Si substrate is removed completely. Selective area wet etching was adopted in order to avoid these effects. The basic idea was to remove a small part of the Si substrate by exposing it to the chemical etching solution, while protecting the rest of the substrate. This allowed for localized strain relaxation, minimizing crack generation. Free-standing LED devices will be obtained after the Si substrate area under the LED devices has been removed by selective wet etching.

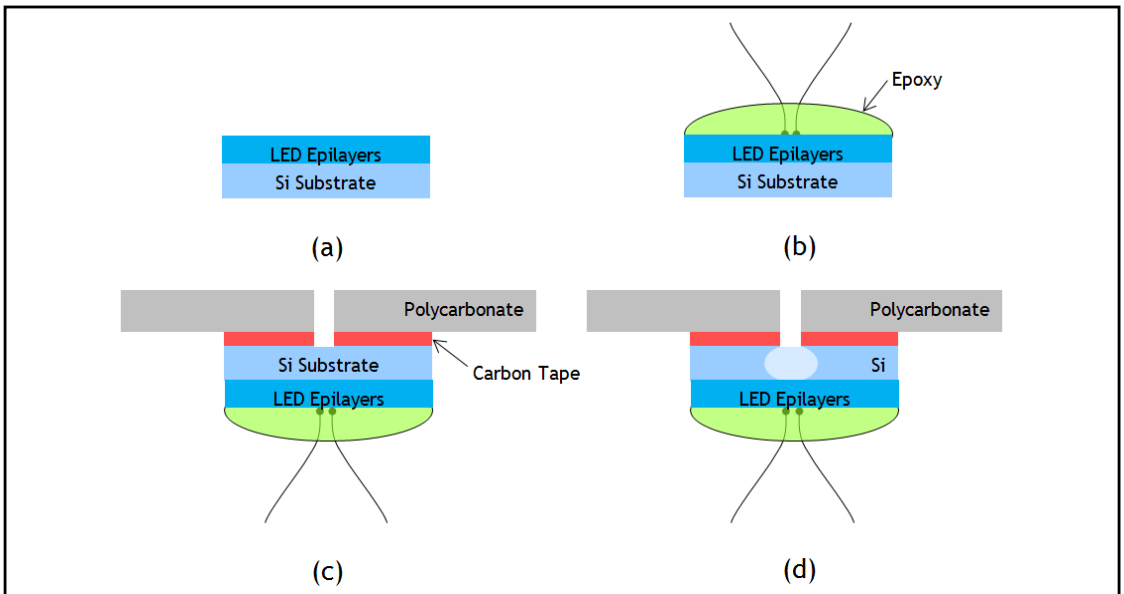


Figure 37: Schematic of selective wet etching process flow: (a) LED epilayers grown on Si (111) substrate by MOCVD, (b) wire bonding on LED device and sealed with epoxy, (c) mount to polycarbonate carrier using carbon tape, and finally (d) silicon substrate selectively removed by wet chemical etching in HNA solution.

In this first phase, conventional device design was used in our LEDs fabrication, in which p-type and n-type contacts are located at the same side of wafer. Epoxy dome sealing was used after the wire bonding of the LED device in order to both stabilize the contact wire and to prevent relaxation-induced film cracking during the Si etch.. Then the assembly was mounted on a polycarbonate plate using double-sided adhesive carbon tape. Vias were drilled in the polycarbonate plates and carbon tape prior to mounting. The process flow is shown in Figure 37. The Si substrate was selectively removed by wet chemical isotropic etching in HNA solution (HNO_3:HF:CH_3COOH = 3:1:1) at room temperature. The etching process can be finished in 3-4 hours for a ~400 μm thick Si substrate. Free-standing LED epilayers were successfully revealed after the etching processes.

Transparent GaN thin films and metal contact pads were clearly observed. However, when LED devices with wire bonding leads were processed in these steps, the device, metal contacts and leads were found to be damaged. It is believed that stress relaxation after the removal of the Si substrate results in warping of the epilayers, causing damage to the LED devices. The presence of cracks could be due to damage caused either during bonding or may be due to strain redistribution during the substrate removal process.

Further, a similar process was repeated, but this time the LED devices were bonded to the Double In-line Package (DIP). Epoxy adhesive glue was used to protect the front side of GaN thin films as well as bonding wires. Vias were drilled in the mount so that the Si substrate can be exposed to the etchant solution, as shown in Figure 38 (a). The mounted LED on Si substrate lit up with 10mA forward drive current, as shown in Figure 38(b). The silicon substrate was selectively removed by wet etching while the chip was mounted in the DIP, which prevented the thin film from cracking or warping. Front and back side image of free-standing GaN LED thin films can be seen in Figure 38(c) and 38(d).

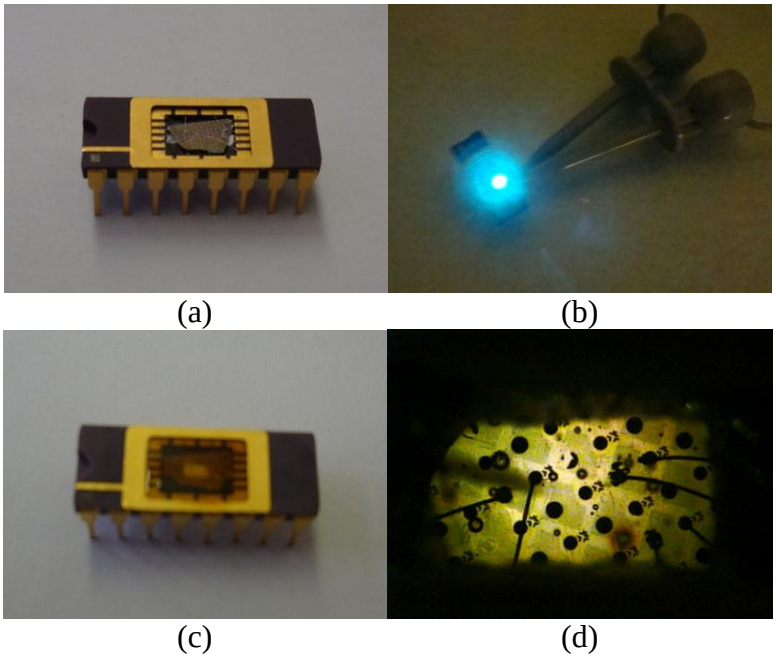


Figure 38: Image of GaN LEDs (a) mounted on ceramic Double In-line Package (DIP) holder by wire bonding, then (b) lit up under forward driving current. (c) Silicon substrate was selectively removed by wet etching, and microscope image of free-standing transparent GaN LED devices from back side.

3.3.2.4 Electrical and optical properties

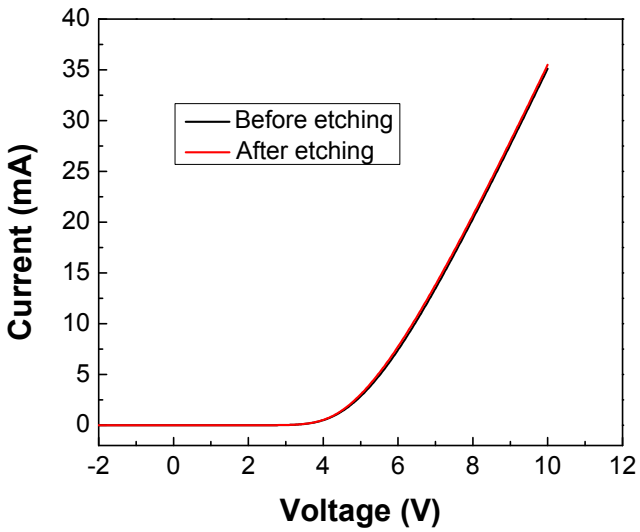


Figure 39: I-V curves for GaN LED on ALD/Si before and after wet etching.

The I-V curves are showed in Figure 39 representing before and after the Si (111) substrate was selectively removed. There is no noticeable difference between the two curves, indicating the removal of silicon substrate does not affect the electrical properties of the LEDs.

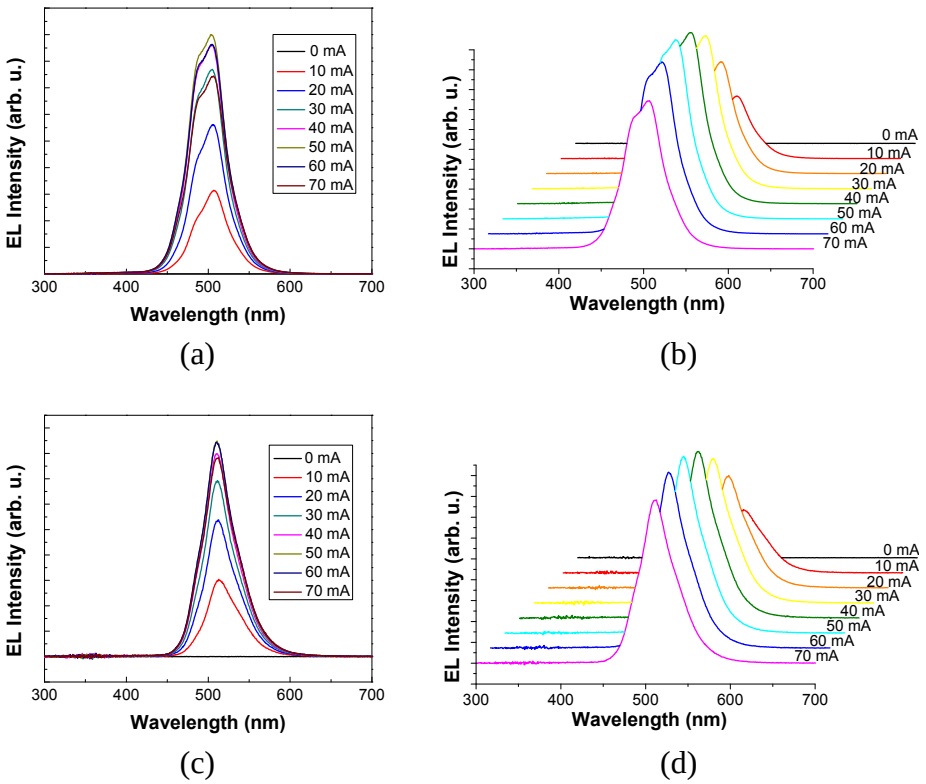


Figure 40: Electroluminescence spectra for GaN LEDs on ALD/Si (a-b) before and (c-d) after wet etching as a function of forward drive current.

Electroluminescence (EL) characteristics of the GaN LED devices grown on ALD/Si were measured before and after the selective removal of Si substrate. EL spectra of the devices as a function of drive current are shown in Figure 40. No significant change in peak emission wavelength shift and EL intensity versus drive current was observed, indicating the modified wet etching process flow was effective to protect the device from being damaged by acid etchant.

Luminescence intensity was also measured as a function of drive current for the same LED devices, and results are shown in Figure 41. The devices before and after wet etching both reach peak luminescence intensity with a drive current of 50~60mA. The efficiency at higher drive current of LEDs after etching was slighter higher than that before etching, which may due to better thermal dissipation after the removal of silicon substrate. However, total radiation flux was reduced, which is due to the absorption by the epoxy adhesive glue on the front side of the device.

As a comparison mentioned above, removal of silicon substrate by simple and cheap wet etching has been achieved, while no degradation of electrical and optical properties was observed.

It could be substantially beneficial to the future substrate transfer and packaging in the industrial fabrication of LED on silicon substrate.

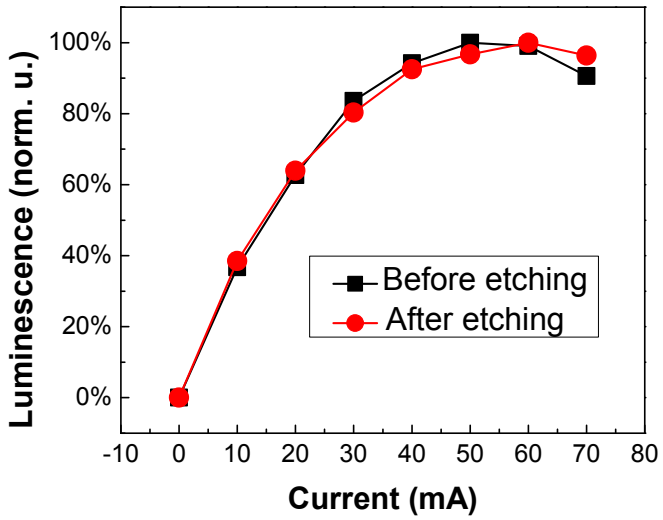


Figure 41: L-I curves for GaN LEDs on ALD/Si before and after wet etching.

3.3.3 Challenges and future outlook

The above process demonstrates the successful removal of the Si substrate for small areas. However, for the large area utilization of substrates the following process (Figure 42) was investigated. After the LED epilayers were epitaxially grown on the Si (111) substrate, ohmic contacts to the p-layer and reflection coating layer metals were deposited on top of the thin film. Then the structure was flipped and bonded onto the Au-plated copper carrier, which can act as both an electric interconnect and thermal spreading pathway. Ultimately the silicon substrate was removed by wet chemical etching in order to make contacts to the n-layer.

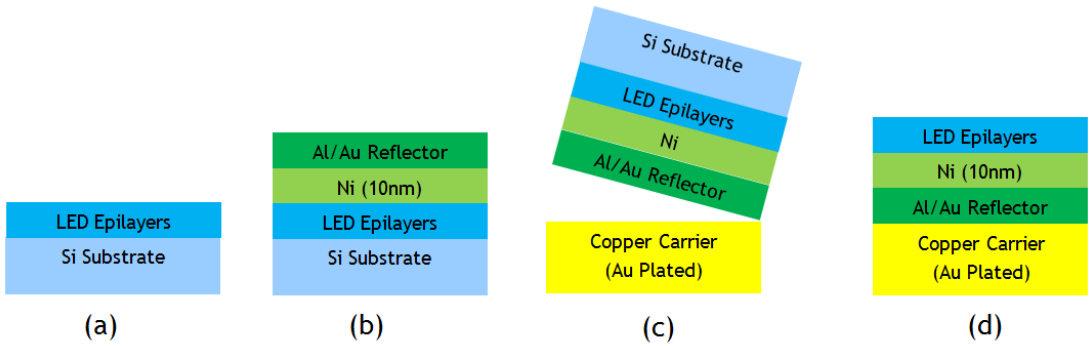


Figure 42: Schematic of substrate removal process flow: (a) Growth of LED epilayers on Si substrate, (b) ohmic contact and reflection layer metal deposition, (c) transfer and bonded to Au plated copper carrier, (d) and finally the removal of Si substrate by wet chemical etching.

However, the mechanical stacking of copper carrier and LED epilayers on Si through interfacial bonding was found to be not fully resistant to the wet-etch solution, making it very difficult to uniformly expose the entire epilayer. Thus this substrate removal process requires a great deal of additional optimization. Also, the lack of an acid resistant and electrically conductive epoxy or other bonding agent further complicated the process. It was also observed that external force introduced during any device fabrication process step, such as bonding of the thin film to the copper carrier, can crack the fragile GaN thin film, thus providing pathways for the acid solution to etch the bonding agent. These challenges in the substrate transfer process need to be overcome before metal contacts to the n-GaN layer can be fabricated from the back side of the LED epilayers.

4. Conclusion

MOCVD growth processes have been developed for GaN on both ZnO and Si substrates using an ALD-grown Al_2O_3 interlayer. Material quality – on Si in particular – is approaching typical values for GaN on sapphire. The process developed in the first part of this work was used to grow crack-free GaN-based LEDs on Si(111) substrates. These $In_xGa_{1-x}N$/GaN MQW LEDs were studied to compare the IQE of devices on Si to comparable devices on sapphire. A comparison of similar LEDs on sapphire and Si reveals several points that show promise toward high-efficiency GaN-based LEDs on Si substrates:

1) Higher efficiency at high drive currents, Fig. 30
2) Similar IQE (>30% at 500nm) to GaN on sapphire, Fig. 31
3) Stable emission wavelength for varying drive currents, Fig. 35

These properties show promise for high-efficiency GaN-based LEDs on silicon substrates. A full industrial-based cost of ownership model shows that using a silicon substrate results in a reduction of ~33% in yielded cost of LED wafers ($28.26 to $18.84) which is a significant cost reduction as required in the DOE SSL Multi-Year Program Plan (MYPP). However, Si substrate removal process by wet etching and transfer of GaN based devices to copper carrier or other heat sinks is still challenging and would need further investigation in the future. The funding for this project has resulted in over 16 refereed journal and conference publications, several conference presentations, and two PhD dissertations.

5. Refereed Journal and Conference Publications

1. W. E. Fenwick, A. Melton, T. Xu, N. Li, C. Summers, M. Jamil, I. T. Ferguson, "Metalorganic chemical vapor deposition of crack-free GaN-based light emitting diodes on Si (111) using a thin Al_2O_3 interlayer", *Appl. Phys. Lett. 94, 222105 (2009). Also featured in the Compound Semiconductor Magazine, July 2009.*
2. W. E. Fenwick, N. Li, T. Xu, A. Melton, S. Wang, H. Yu, C. Summers, M. Jamil, and I. T. Ferguson, "MOCVD Growth of GaN on Si(111) substrates using an ALD-grown Al_2O_3 interlayer" *J. Crystal Growth, 311, 4305 (2009).*
3. Nola Li, Shen-Jie Wang, Eun-Hyun Park, Zhe Chuan Feng, Hung-Lin Tsai, Jer-Ren Yang, and Ian Ferguson, "Suppression of phase separation in InGaN growth on ZnO substrates compared to growth on sapphire" *J. crystal growth,* 311, 4628 (2009).

4. S.-J. Wang, N. Li, H. Yu, Z. Chuan, A. Valencia, J. Nause, C. Summers, and I. Ferguson "Metalorganic Chemical Vapor Deposition of GaN Layers on ZnO Substrates using α-Al_2O_3 as a Transition Layer" Journal of Physics D: Applied Physics, 42, 245302 (2009).

5. N. Li, S.-J. Wang, C.-L. Huang, Z. C. Feng, A. Valencia, J. Nause, C. Summers, and I. Ferguson "Effect of an Al_2O_3 Transition Layer on InGaN on ZnO Substrates by Organometallic Vapor Phase Epitaxy", J. of Crystal Growth, 310, 4908 (2008).

6. N. Li, S.-Jie Wang, E.-H. Park, Z. C. Feng, A. Valencia, J. Nause, C. Summers, and I. Ferguson, "Influence of High Indium Composition InGaN on Lattice Matched ZnO Sacrificial Substrates", Journal of Light & Visual Environment, 32(2), 143 (2008).

7. S.-J. Wang, N. Li, E.-H. Park, Z. C. Feng, A. Valencia, J. Nause, M. Kane, C. Summers, and I. Ferguson, "MOCVD growth of GaN-based materials on ZnO substrates", physica status solidi (c), 5(6), 1736 (2008).

8. W.E. Fenwick, N. Li, M. Jamil, T. Xu, A. Melton, S. Wang, H. Yu, A. Valencia, J. Nause, C.Summers, I.T. Ferguson, "Development of new substrate technologies for GaN LEDs: atomic layer deposition transition layers on silicon and ZnO", *Proc. of SPIE, Vol. 7231 723119-1 (2009).*

9. N. Li, W. Fenwick, A. Melton, I-H. Hung, Z. C. Feng, C. Summers, M. Jamil, and I. Ferguson, "III-Nitride Epilayers on ZnO Substrates by MOCVD Using Al_2O_3 as a Transition Layer" *Proc. of SPIE, Vol. 7422, 74220J-1 (2009).*

10. N. Li, S.-J. Wang, A. Valencia, J. Nause, C. Summers, and I. Ferguson, "Metalorganic Vapor Deposition of GaN and InGaN on ZnO Substrate using Al_2O_3 as a Transition Layer", Proceedings of the International Society for Optical Engineering (SPIE) 7058, (70580K), (2008).

11. N. Li, S.-J. Wang, C.-L. Huang, Z. C. Feng, A. Valencia, J. Nause, C. Summers, and I. Ferguson, "Effect of an Al_2O_3 Transition Layer on InGaN on ZnO Substrates by OMVPE", 14th International Conference of Metalorganic Vapor Phase Epitaxy, Metz, France, June 2008.

12. N. Li, S.-J. Wang, A. Melton, C.-L. Huang, Z. C. Feng, A. Valencia, J. Nause, C. Summers, and I. Ferguson, "Al_2O_3 as a Transition Layer for GaN and InGaN Growth on ZnO by MOCVD", 5th International Workshop on ZnO and Related Materials, Michigan, USA, Sept. 2008.

13. W. E. Fenwick, M. Jamil, T. Xu, S. Wang, H. Yu, A. Melton, N. Li, J. Nause, and I. T. Ferguson, "MOCVD Growth of GaN-based Materials on ZnO and Si Substrates", Materials Research Society Symposium Proceedings, 1109E (1109-B08-10), 2009.

14. N. Li, S.-J. Wang, J. Nause, A. Valencia, C. Summers, I. Ferguson, "InGaN layers grown on passivated Al_2O_3/ZnO substrates prepared by atomic layer deposition", MRS Symposium Proc.1035E(1035-L11-23), 2008.

15. C.L. Huang, Y.Z. Huang, Z.C. Feng, Y.L. Shen, N. Li, S.J. Wang and I. Ferguson, "Optical and structure properties of MOCVD-grown InGaN/GaN on ZnO substrate with Al_2O_3 transition layer by atomic layer deposition", Taiwan Display Conference, Taipei, Taiwan, 2008, p. 383-386.

16. N. Li, S.-J. Wang, W. Fenwick, A. Melton, C.-L. Huang, Z. C. Feng, C. Summers, M. Jamil, and I. Ferguson, "Al_2O_3 as a Transition Layer for GaN and InGaN growth on ZnO by MOCVD", Materials Research Society Symposium Proceedings, 2010.

Invited Keynote Addresses/Special Presentations:

(**Invited)** N. Li, W. E. Fenwick, T. Xu, A. Melton, S.-J. Wang, H. Yu, C. Summers, M. Jamil, I. T. Ferguson, "ALD Sapphire Transition Layer to Create a Universal Substrate on Silicon and ZnO", 2nd International Conference on White LEDs and Solid State Lighting, Taipei, Taiwan, 2009.

Conference Presentations without Proceedings:

You-Ren Lan, Zhe-Chuan Feng, Nola Li, Ian Ferguson, Weijie Lu, "Second Ion Mass Spectroscopy for Surface and Structural Investigation of InGaN/GaN on ZnO Substrate", 2nd International Conference on White LEDs and Solid State Lighting, Taipei, Taiwan, Dec. 2009.

Yee Ling Chung, Zhe Chuan Feng, Lin Li, Shude Yao, Nola Li, Ian T. Ferguson, Weijie Lu, and Tao Fa, "Rutherford Backscattering Analysis of InGaN/GaN Structures Grown on ZnO substrate", 2nd International Conference on White LEDs and Solid State Lighting, Taipei, Taiwan, Dec. 2009.

Nola Li, Will Fenwick, Zhe Chuan Feng, Christopher Summers, Muhammad Jamil, and Ian Ferguson, "Atomic Layer Deposition of Al_2O_3 as a Transition Layer for III-Nitride Epilayers on ZnO Substrates", 4th Asia-Pacific Workshop on Widegap Semiconductors, Zhangjiajie, Hunan, China, May 2009.

William E. Fenwick, Muhammad Jamil, Nola Li, Andrew Melton, Tianming Xu, Shenjie Wang, Hongbo Yu, Jeff Nause, and Ian T. Ferguson, "MOCVD growth of GaN on Si(111) substrates using an ALD-grown Al_2O_3 interlayer", Department of Energy Workshop, San Francisco, CA, USA, Feb. 2009.

Nola Li, Shen-Jie Wang, Chung-Lung Huang, Zhe Chuan Feng, Adriana Valencia, Jeff Nause, Christopher Summers, and Ian Ferguson, "Al_2O_3 as a Transition Layer for MOCVD Growth of GaN and InGaN on ZnO Substrates", UK Semiconductors, University of Sheffield, 2008.

Nola Li, Shen-Jie Wang, Hongbo Yu, Christopher Summers, and Ian Ferguson, "InGaN Growth on ZnO Substrate by MOCVD", Georgia Institute of Technology Graduate Student Symposium, Atlanta, GA, USA 2008.

Nola Li, Shen-Jie Wang, Hongbo Yu, Vincent Woods, Christopher Summers, and Ian Ferguson, "Epitaxial Growth of GaN Based LEDs on Simple Sacrificial Substrates", Department of Energy Workshop, Atlanta, GA, USA, Jan. 2008.

Tianming Xu, et al., Numerical and experimental study of ZnO thin film grown by MOCVD, presented at the 6th International Workshop on Modeling in Crystal Growth (2009).

6. APPENDIX: Cost of Ownership Model Using Si Substrates for LED Growth

A cost of ownership model has been developed for current EMCORE E300 technology and new Applied Materials (AM) tool that is currently operational in TSMC (Epistar) in Taiwan. The Epistar/AM tool can grow on 52 wafers/growth run resulting in ~3150 wafers per week with a estimated cost of ~$28/wafer including the substrate. The cost per wafer for the E300 tool of $43.66 reduces to cost per wafer of $28.26 for the AM tool using similar variables. The estimated close cost of the epitaxial material is now close to the industry metric of about 1.5x the wafer cost. Additional cost savings can now only be made with reduction in the cost of the substrate material. Using an equivalent cost per square inch for silicon results in a factor of four (4) reduction in the substrate costs. A full CoO model shows that using a silicon substrate results in a reduction of ~33% in yielded cost of LED wafers ($28.26 to $18.84).

Table 14: Cost associated with operating time of a production MOCVD growth system.

System Process Wafer Size	**E300** **LED (Sapphire)** 2"	**AM (52 wafers)** **LED (Sapphire)** 2"	**AM (52 wafers)** **LED (Silicon)** 2"
Desired thickness (um)	2.30	2.30	2.30
Deposition rate (um/hr)	1.90	1.90	1.90
Deposition time (hr)	**1.21**	**1.21**	**1.21**
Time to temperatures (up and down) (hr)	0.40	0.40	0.40
Time to load (hr)	0.02	0.02	0.02
Time to unload (hr)	0.02	0.02	0.02
Loadlock cycle/purge time/run (hr)	0.05	0.05	0.05
Time to purge/vent (hr)/conditioning	0.00	0.00	0.00
Overhead time (hr)	**0.49**	**0.49**	**0.49**
Hours per week per shift	40	40	40
Shifts per week	3	3	3
Weeks per year	50	50	50
Time in year (hr/year)	**6,000**	**6,000**	**6,000**
Wafers per run	19	52	52
Number of runs per year	**3,528**	**3,528**	**3,528**
Gross throughput (wafers)	**67,038**	**183,473**	**183,473**
Time between reactor cleans (hr)	900	900	900
Time to clean and requal (hr)	16	16	16
% time down to clean	**1.75%**	**1.75%**	**1.75%**
Preventative maintenance interval (hr)	600	600	600
Clean time during PM (hr)	1	1	1
Requal. time during PM (hr)	0	0	0
% time down for PM	**0.17%**	**0.17%**	**0.17%**

Table 15: Other costs and yield percentages for MOCVD production systems.

System	E300	AM (52 wafers)	AM (52 wafers)
Process	LED (Sapphire)	LED (Sapphire)	LED (Silicon)
Wafer Size	2"	2"	2"
Repair time (hr)	4	4	4
Response time (hr)	1	1	1
Requalification time (hr)	3	3	3
Mean time between failures (hr)	1,000	1,000	1,000
% time down for repairs	**0.80%**	**0.80%**	**0.80%**
% assist. time	0.75%	0.75%	0.75%
total % time down	**3.46%**	**3.46%**	**3.46%**
Net throughput (wafers)	**64,716**	**177,118**	**177,118**
Utilization rate	96%	96%	96%
Effective number of runs/year	**3,270**	**3,270**	**3,270**
Non product runs, cal/test/coat (%)	3%	3%	3%
Number of product runs/year	**3,172**	**3,172**	**3,172**
Gross product wafers out/year	**60,264**	**164,932**	**164,932**
Product yield (% good wafers)	97%	97%	97%
Effective throughput (wafers)	**58,456**	**159,985**	**159,985**
User defined wafers out (good wafer/wk)	1,150	3,150	3,150
Calculated Systems Required	**0.98**	**0.98**	**0.98**
Total systems for wafer demand	**1**	**1**	**1**

Table 16: Substrate and system costs for MOCVD production systems.

System	E300	AM (52 wafers)	AM (52 wafers)
Process	LED (Sapphire)	LED (Sapphire)	LED (Silicon)
Wafer Size	2"	2"	2"
Capital for basic system(s) ($)	$1,600,000.00	$3,000,000.00	$3,000,000.00
Facilitation costs ($)	**$160,000.00**	**$300,000.00**	**$300,000.00**
Total capital required ($)	**$1,760,000.00**	**$3,300,000.00**	**$3,300,000.00**
Time to depreciate (years)	7	7	7
Annual depreciation ($/year)	**$251,428.57**	**$471,428.57**	**$471,428.57**
Required floor space (sq. meter)	26.00	26.00	26.00
Cost per square meter ($/sq.m/month)	$30.00	$30.00	$30.00
Average Power required (kw.hr)	30.00	30.00	30.00
Cost per kilowatt hour ($/kw.hr)	$0.10	$0.10	$0.10
Number of operators required/system	0.50	0.50	0.50
Operator's Salary + Overhead ($/hr)	$15.00	$15.00	$15.00
Cost of epi materials ($/run)	$400.00	$600.00	$600.00
Operating Cost @ full utilization ($)	**$1,378,991.56**	**$2,032,966.58**	**$2,032,966.58**
Total Annual Operating Cost ($)	**$1,630,420.13**	**$2,504,395.15**	**$2,504,395.15**
For required number of systems			
CPWP @ full utilization	**$27.89**	**$15.65**	**$15.65**
CPWP @ user rate	**$27.97**	**$15.70**	**$15.70**
Cost of substrate wafer ($)	$15.00	$12.00	$3.00
Yielded cost of wafer ($)	**$15.70**	**$12.56**	**$3.14**
CPWP + Substrate @ full utilization	**$43.59**	**$28.21**	**$18.79**
CPWP + Substrate @ user rate	**$43.66**	**$28.26**	**$18.84**

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